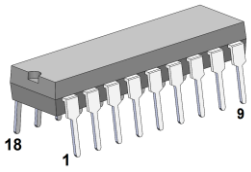
AS3320 - Voltage controlled filter (VCF)

FEATURES

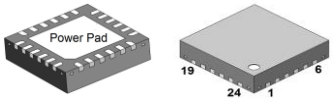
- voltage controllable frequency - 12 octave range
- voltage controllable resonance - from zero to oscillation
- accurate exponential frequency scale
- accurate linear resonance scale
- low control voltage feedthrough -45dB typical
- filter configurable into LPF, HPF, all pass, etc.
- low noise: -86dB typical
- low distortion in passband - 0.1% typical
- low warm up drift
- configurable into low distortion voltage controlled sine wave oscillator
- bandwidth till 800kHz

APPLICATIONS
for electronic music

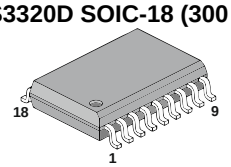
AS3320
PDIP-18 (300 mil)



AS3320F
QFN-24 4x4mm 0,5mm



AS3320D SOIC-18 (300 mil)



General Description

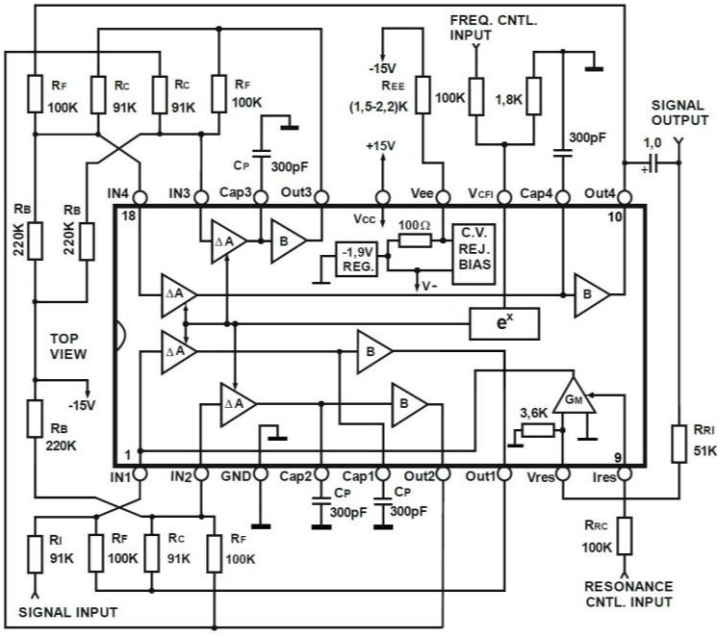
The AS3320 is a high performance voltage controlled four-pole filter with on-chip voltage controllable resonance IC. The four independent sections may be interconnected to provide a wide variety of filter responses, such as low pass, high pass, band pass and all pass. A single input exponentially controls the frequency over greater than a ten octave range with little control voltage feedthrough. Another input controls the resonance in a modified linear manner from zero to low distortion oscillation. For those demanding applications, provision has been made to allow trimming for improved control voltage rejection. Each filter section features a variable gain cell which is fully temperature compensated, exhibits a better signal-to-noise ratio and generates its low distortion predominantly in the second harmonic. The device includes a minus two volt regulator to ensure low power dissipation and consequent low warm-up drift.

Power pad in QFN package highly improves thermal stability of parameters of AS3320F.

Pin Information

PDIP-18, SOICW-18 Pin No	QFN-24L Pin No	Pin Name	Description
1	4	IN1	Input Stage 1
2	5	IN2	Input Stage 2
3	7	GND	Ground
4	8	Cap2	Capacitor Stage 2
5	9	Cap1	Capacitor Stage 1
6	11	Out2	Output Stage 2
7	12	Out1	Output Stage 1
8	14	Vres	Resonance Input
9	15	Ires	Resonance Control Input
10	16	Out4	Output Stage 4
11	17	Cap4	Capacitor Stage 4
12	19	V_{CFI}	Voltage Control Frequency Input
13	20	Vee	Negative power
14	22	Vcc	Positive power
15	23	Out3	Output Stage 3
16	24	Cap3	Capacitor Stage 3
17	2	IN3	Input Stage 3
18	3	IN4	Input Stage 4
-	Power pad	Power pad	Don't connect

Circuit Block and Connection Diagram (PDIP-18, SOIC-18)



Absolute Maximum Ratings

Voltage between Vcc and Vee pins	+22V, -0,5V
Voltage between Vcc and GND pins	+18V, -0,5V
Voltage between Vee and GND pins	-4V, -0,5V
Voltage between Cell Input and GND pins	+0,5V, -6V
Voltage between Frequency Control and GND pins	±6V
Voltage between Resonance Control and GND pins	+2V, -18V
Current through any pin	±40mA
Storage Temperature Range	- 55°C to 150°C
Operating Temperature Range	- 25°C to 75°C

Electrical Characteristics *

V_{CC}=+15V R_F = 100K T_A= 25°C

Parameter	Min.	Typ.	Max.	Units
Gain of Variable Gain Cell at V_{CFI}=0	0.7	1	1,3	
Input Bias Current of Frequency Control Input	0.2	1	1.5	μA
Input Impedance of Resonance Signal Input	2.7	3.6	4.5	K Ω
Output Swing At Clipping	10	12	14	V.P.P.
Output voltage DC [1]	5	6.5	9	V
Buffer Input Bias Current	±10	±30	±100	nA
Buffer Output Impedance [2]	25	50	100	Ω
Voltage at the negative supply pin [3]	-2.4	-2.7	-2.9	V
Positive Supply Current, I_{CC}	3.8	5	6.5	mA
Negative Supply Current, I_{EE} [3]	8	8.4	8.8	mA

Typical Electrical Characteristics

Parameter	Min.	Typ.	Max.	Units
Pole Frequency Control Range [4]	3500:1	10,000:1	-	
Sensitivity of Pole Frequency Control Scale, Midrange	57.5	60	62.5	mV/decade
Tempco of Pole Frequency Control Scale	3000	3300	3600	ppm
Exponential Error of Pole Frequency Control Scale[5]	-	4	12	%
Max Gain of Variable Gain Cell	2.4	3	3.6	
Tempco of Variable Gain Cell [6]	-	500	1500	ppm
Output Impedance of Gain Cell [6]	0.5	1	2	MΩ
Pole Frequency Control Feedthrough	-	60	200	mV
Pole Frequency Warm-up Drift	-	0.5	1.5	%
Gm of Resonance Control Element at I_{CR}=100μA	0.8	1	1.2	mmhos
Amount of Resonance Obtainable Before Oscillation	20	30	-	dB
Resonance Control Feedthrough [7]	-	0.2	1,5	V
Output Noise re Max Output [8]	-76	-86	-	dB
Rejection in Bandreject	73	83	-	dB
Distortion in Passband [9,11]	-	0.1	0.3	%
Distortion in Bandreject [10,11]	-	0.3	1	%
Distortion of Sine Wave Oscillation [12]	-	0.5	1.5	%
Internal Reference Current, I_{REF}	45	63	85	μA
Buffer Slew Rate	1.5	3	-	V/μS
Buffer Sink Capability	0.4	0.5	0.63	mA
Positive Supply Range, V_{CC}	+9	-	+18	V
Negative Supply Range, V_{EE} [3]	-4	-	-18	V

***) Specifications subject to change without notice.**

Note 1: V_{IN} = 0, R_C = 91KΩ, R_F = 100KΩ
Note 2: V_{CFI} = 0
Note 3: Current limiting resistor always required. R_{EE} = (15V – 2.7V)/ 8.4 mA ~ 1.5k for negative supply -15V
Note 4: -20mV < V_{CFI} < +160mV
Note 5: -16mV < V_{CFI} < +176mV. Most of this error occurs in upper two octaves.
Note 6: V_{CFI} = 0
Note 7: Untrimmed. 0 < I_{CR} < 100μA
Note 8: Filter is connected as low pass and set for 20 KHz cut-off frequency.
Note 9: Output signal is 3dB below clipping point.
Note 10: Output signal is 3dB below passband level, which is 3dB below clipping point. In general, this is worst case condition.
Note 11: Distortion is predominantly second harmonic.
Note 12: Sinewave is not clipped by first stage.

Typical Application - VCF Circuits

For application solutions from Fig. 1, Fig. 2, Fig. 3, Fig. 4:

1. VEE = -15V Ree = (15 - 2.7) / 0.008=1537 Ohm (1.5K),
   VEE = -12V Ree = (12 - 2.7) / 0.008=1162 Ohm (1.2K),
   VEE = -10V Ree = (10 - 2.7) / 0.008= 910 Ohm
2. All resistors for Vcc +10V and +12V remains the same, except Rb must be changed from 220K to 240K
3. For maximum AC voltage on filter out, DC voltage on the output of each stage should be kept ~ 0.45 * +Vcc

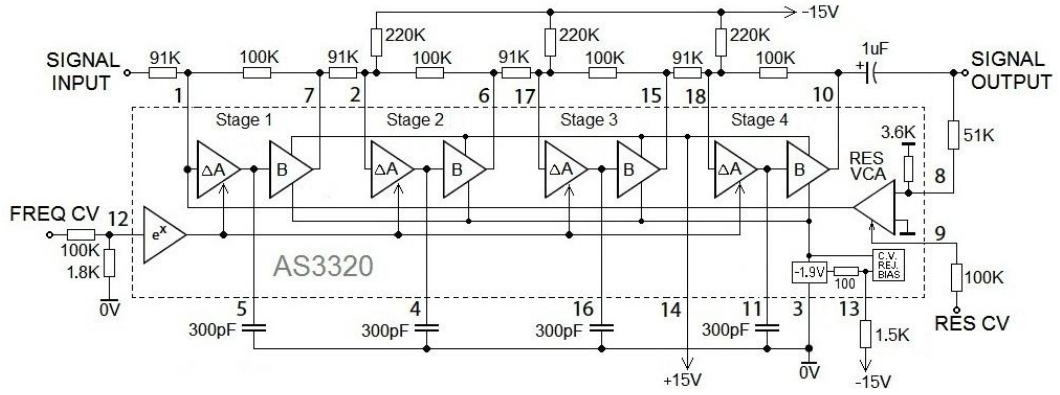


Figure 1. Low Pass Filter Circuit

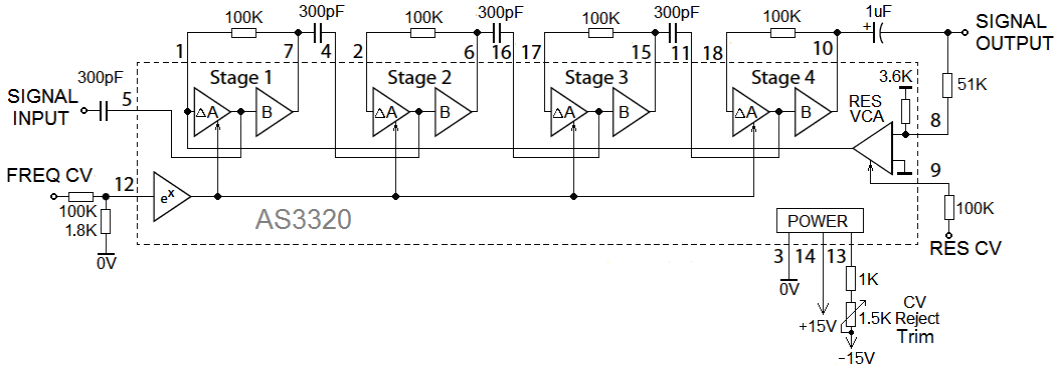


Figure 2. High Pass Filter Circuit

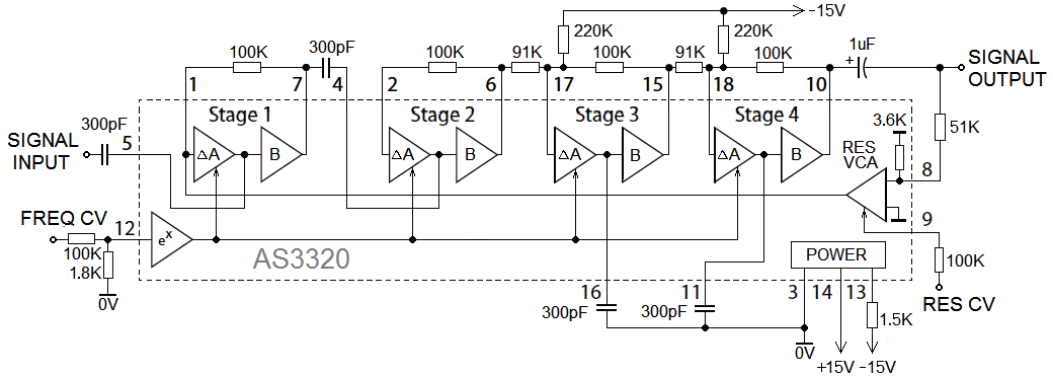


Figure 3. Band Pass Filter Circuit

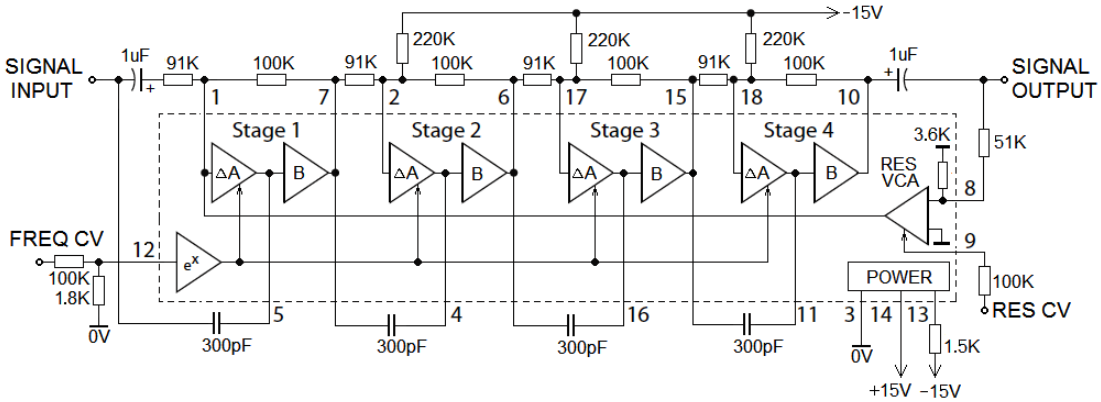
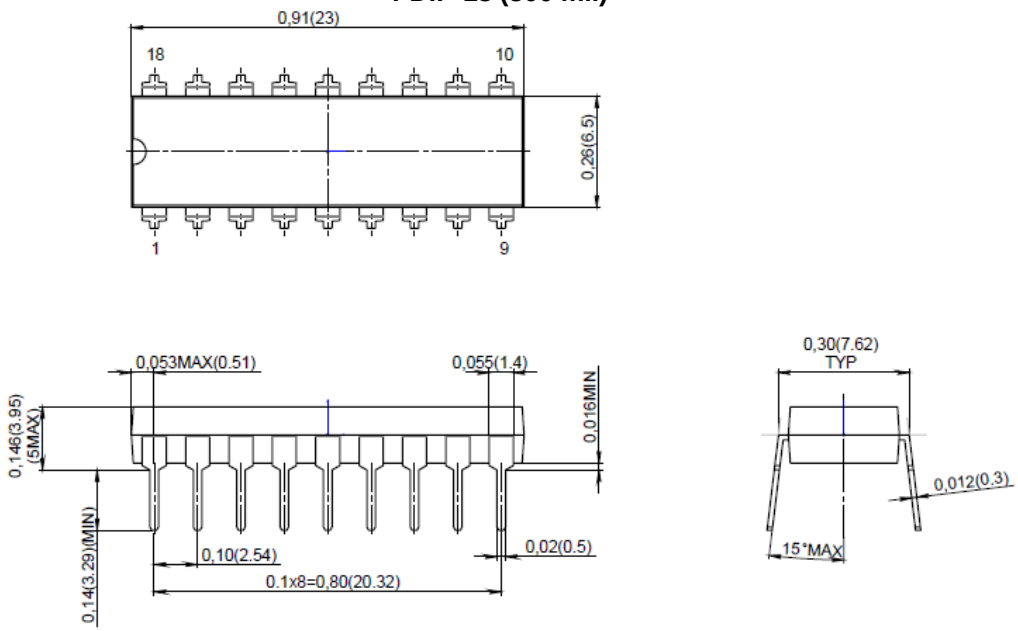


Figure 4. All Pass Filter Circuit

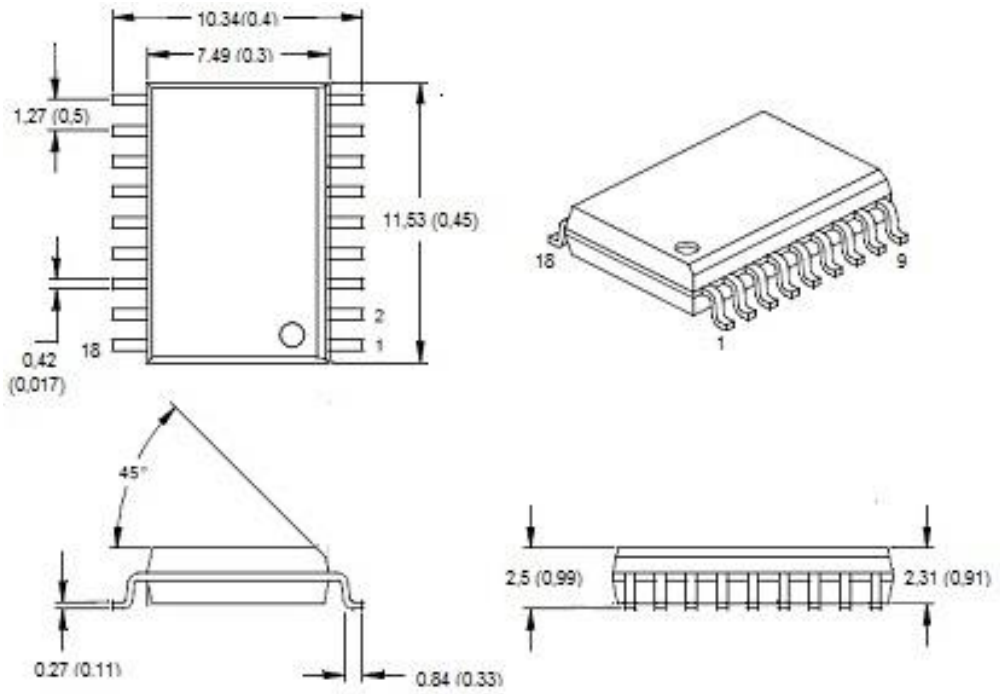
Device type	Package
AS3320	PDIP-18 (300 mil body)
AS3320D	SOIC-18 (300 mil body)
AS3320F	QFN-24L (4*4 mm 0.5 mm)

Package Information

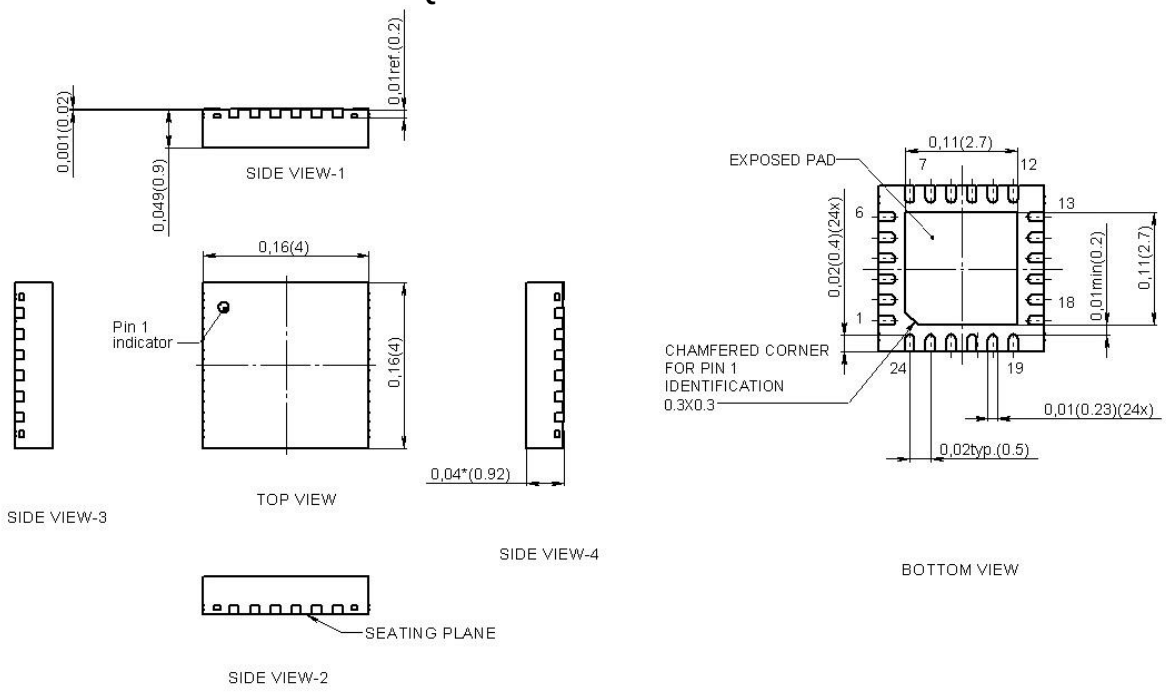
PDIP-18 (300 mil)



SOIC-18 (300 mil)



QFN-24 4x4 mm 0.5 mm



Revision history

Date	Revision	Changes
05-Oct-2016	**1**	Short version 1
09-Jan-2017	**2**	QFN-24L – new package
20-Mar-2017	**3**	Drawing and typical electrical characteristics updated
09-May-2017	**4**	Block circuit and typical electrical characteristics updated
29-May-2017	**5**	Minor changes
21-May-2018	**6**	Minor changes
10-Jun-2019	**7**	SOICW-18L – new package
27-May-2020	**8**	Note 3 correctIon
06-Feb-2023	**9**	Application note included
07-Feb-2023	**10**	Minor changes, corrections