



## AS3364 – Quad Voltage Linearly Controlled Amplifier (VCA)

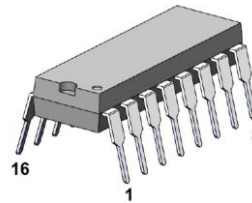
### FEATURES

- "Linear replacement" – "pin compatible" to AS2164
- Exceptionally low control feedthrough without trimming: 10mV maximum out of 10 V.P.P. output
- Low noise: -110 dB typical
- Summing node signal Inputs
- Current outputs capable of swinging to within 1,5V of each supply
- Control voltages referenced to ground
- Wide supply range:  $\pm 3$  to  $\pm 12$ V or +15, -3 to -9V

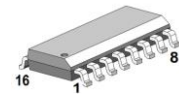
### APPLICATIONS

for electronic music

AS3364  
PDIP-16 (300 mil)



AS3364D  
SOIC-16 (150 Mil)



### General Description

The AS3364 is a quad general purpose voltage linearly controlled VCA intended for such applications as voltage controlled amplifiers, filters, and waveform generators. Each VCA independently provides linear control scaling over greater than a 100 dB range. Complete with virtual ground summing inputs, wide voltage compliance current outputs, and control inputs referenced to ground, the AS3364 requires exceptionally few external components and is extremely easy to use.

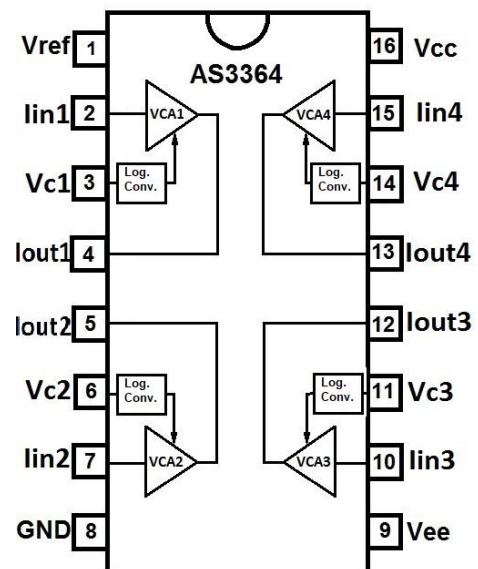
Because of its inherent ultra-low control feedthrough, no trimming is required. Added to these features are exceptionally low noise, wide bandwidth, and operation down to  $\pm 3$  volts, making the AS3364 a real cost saver in most applications requiring variable transconductance amplifiers.

AS3364 pinout allows simple replacement of AS2164 (adding just one capacitor to Vref) witch simplify circuit design with linear control.

### Pin Information

PDIP-16, SOIC-16	Pin Name	Description
1	Vref	Reference Voltage Output
2	lin1	Current Input 1
3	Vc1	Linear Control Input 1
4	lo1	Current Output 1
5	lo2	Current Output 2
6	Vc2	Linear Control Input 2
7	lin2	Current Input 2
8	GND	Ground
9	Vee	Negative Supply
10	lin3	Current Input 3
11	Vc3	Linear Control Input 3
12	lo3	Current Output 3
13	lo4	Current Output 4
14	Vc4	Linear Control Input 4
15	lin4	Current Input 4
16	Vcc	Positive Supply

### Functional diagram





**Absolute Maximum Ratings**

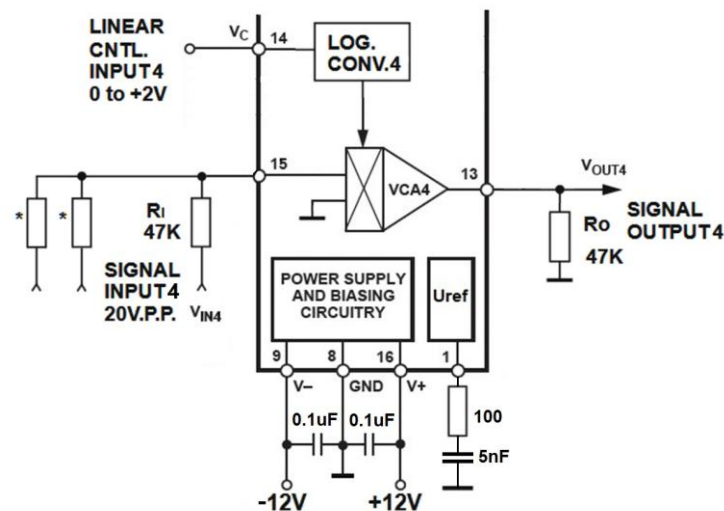
Voltage Between $V_{CC}$ and $V_{EE}$ Pins	26V
Voltage Between $V_{CC}$ and GND Pins	+3V to +16V
Voltage Between $V_{EE}$ and GND Pins	-3V to -16V
Linear Control Voltage	-2V to +2,5V

**Typical Electrical Characteristics**  
 $V_{CC} = +12.0V$   $V_{EE} = -12.0V$   $T_a = 20^\circ C$

Parameter	Min	Typ	Max	Units
Control Range, linear	100	-	-	dB
Control Scale Factor, linear	48	52	56	%/V
Tempco of Control Scales	-	$\pm 250$	$\pm 750$	ppm
Control Scale Error 1)	-	3,0	6,0	%
Maximum Cell Current Gain 2)	0,9	1,0	1,1	
Maximum Signal Input and Output Current	$\pm 300$	$\pm 400$	$\pm 500$	$\mu A$
Signal Input Offset	-10	0	+10	mV
Control Feedthrough, trimmed 3)	-	$\pm 0,07$	$\pm 0.3$	$\mu A$
Total Harmonic Distortion 3)	-	1,0	3,0	%
Output Noise Current 4)	-	0,4	1,2	nA
Signal Current Bandwidth	2,0	5,0	-	MHz
Signal Current Slew Rate 2)	0,5	1,5	-	$mA/\mu sec$
Crosstalk Between VCAs 5)	-80	-90	-	dB
Signal Attenuation for Linear Control Input = 0V 6)	70	80	-	dB
Linear Control Voltage for Maximum Gain	1,79	1,93	2,08	V
Control Input Bias Current	-0,5	-1,6	-4,0	$\mu A$
Output Impedance 2)	5	12	-	MOhm
Output Voltage Compliance 2)	$V_{EE}+1,2$	-	$V_{CC}-0,8$	V
Reference Voltage (Pin 1)	1,7	1,8	1,9	V
Positive Supply Voltage Range 7)	+3	-	+16	V
Negative Supply Voltage Range 7)	-3	-	-16	V
Supply Current	6	7,5	10,0	mA

- Note 1. Best linearization. Most of the error at the ends of diapason.  
 Note 2. Output current  $\pm 100\mu A$ .  
 Note 3. Over entire control range. Signal input is open  
 Note 4. In 16 to 16KHz bandwidth.  
 Note 5. At 1KHz.  
 Note 6. For negative supply less than 12 volts, this attenuation is greater.  
 Note 7. Total supply voltage across chip should not exceed 26V.  
**Specifications subject to change without notice**

**Application example**



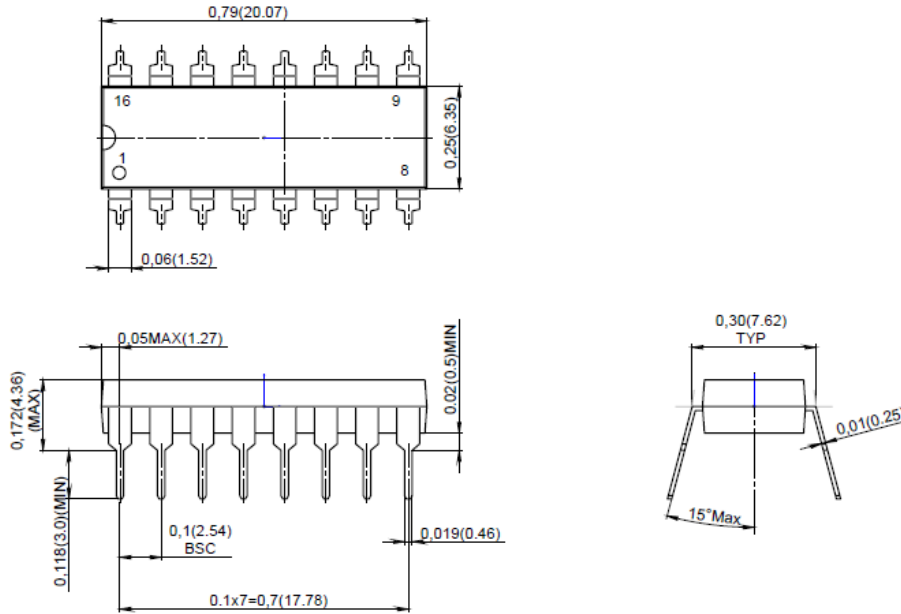


Package Information

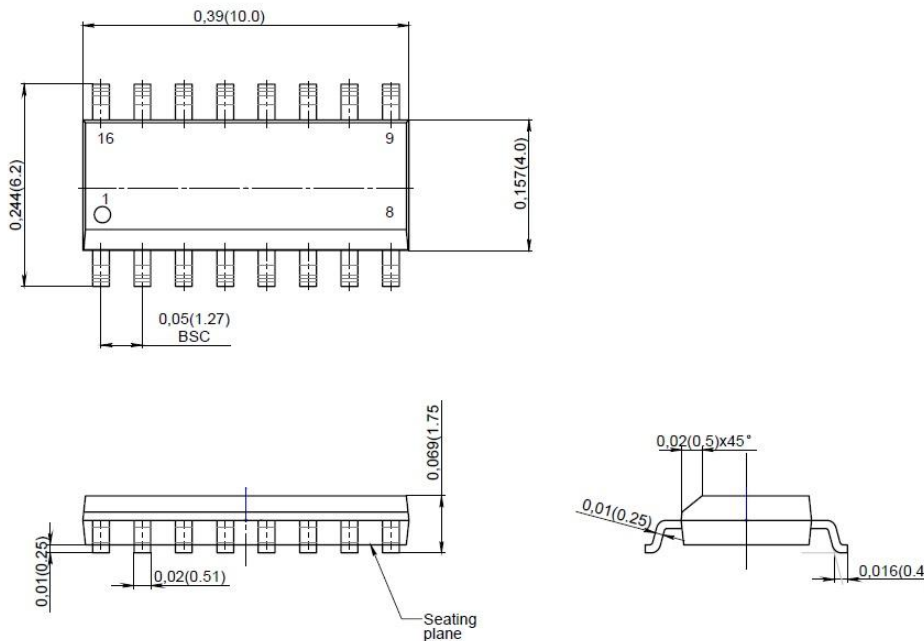
Device type	Package
AS3364	PDIP-16 (300 Mil)
AS3364D	SOIC-16 (150 Mil)

Units: inch (mm)

PDIP-16 (300 mil)



SOIC-16 (150 mil)



Revision history

Date	Revision	Changes
26-Mar-2019	1	Preliminary version 1
18-Apr-2020	2	PDIP-16 – New package