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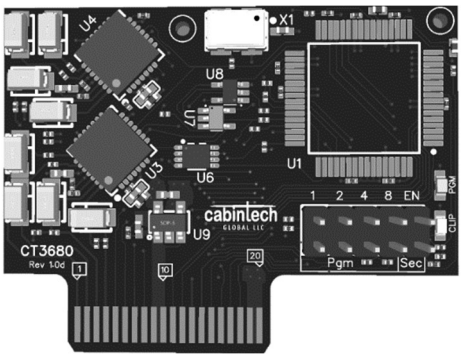
CT3680 Multi-Delay Module V1
Datasheet and Development Guide



The Cabintech CT3680 is a hybrid module that implements from 1 to 4 flexible, configurable audio delay lines that are similar to traditional analog BBD devices such as the MN3xxx series of chips. This module can be used by system designers to create many different delay-based effects (echo, chorus, flanger, etc.) using traditional analog feedback paths, filters, and modulation techniques. Although the CT3680 is digital at its core, all inputs and outputs are analog, no programming or digital logic design is required.

The CT3680 is designed to be easy to use with simple analog audio inputs and outputs, control voltages to set parameter values (such as delay time), and a single +5V power supply. The small module size (23x38mm, 0.9x1.5in) and multiple connector/adapter options provide flexibility for mechanical fitment into small spaces and optimize the use of PCB board space.

From a system design point of view the CT3680 is a set of independent analog delay lines capable of providing up to 682ms of delay and from 1 to 4 “taps”. Each tap is a point in the delay line where the audio signal is extracted and provided on an output pin. The delay time at each tap is independently voltage controlled (e.g. 0.0V produces minimum delay time, 3.3V produces maximum delay time). Minimum and maximum delay times are defined by global scalar CV inputs (see *Setting Delay Times* on page 19). All CV inputs can be modulated to dynamically vary the controlled parameter.

In the default configuration, the CT3680 is a single 682ms delay line with 4 taps. It can also be configured to be 2 independent delay lines (340ms delay and 2 taps each), 3 delay lines (226ms delay, 1 tap each), or 4 delay lines (170ms delay and 1 tap each). Unlike analog BBD modules, the CT3680 does not degrade audio fidelity at longer delay times (the sampling rate is fixed at 48kHz and does not change with delay time). Longer delay times and more channels can be achieved by linking multiple CT3680 modules together.

The CT3680 requires no external clock and is powered by +5V. Note that all analog and CV signals are +3.3V maximum (see *Specifications and Maximum Ratings* on page 6). A +3.3V reference is made available on an output pin. All audio analog inputs and outputs are single-ended, 2.5V full scale, and AC coupled. Clipping is detected and signaled on an output pin and an onboard LED.

This datasheet is for hardware version 1.

Contents

Features

- Input pin selectable configuration for 1, 2, 3, or 4 independent delay lines in multiple configurations.
- Maximum delay of 682ms (divided between all delay lines)
- Minimum delay time of 0.3ms
- 4 CV inputs to control delay and other parameters
- 2 global scalar CVs (min delay, max delay)
- Digitally chainable up to 5 modules with total max delay of 3.4 seconds
- +5V 170mA power supply
- Reverse voltage protection
- 4 analog audio inputs
- 4 analog audio outputs
- Internal digital sampling at 48kHz
- No external clock is required
- Clipping-detected output signal and on-board clipping LED
- Castellated edges for direct soldering to a PCB (through-hole adapter is available)

Pinout

Pin	I/O	Symbol	Description
1	In	AUDIO_IN_1	Audio input 1
2	In	AUDIO_IN_2	Audio input 2
3	Out	AUDIO_OUT_1	Audio (tap) output 1
4	Out	AUDIO_OUT_2	Audio (tap) output 2
5	-	N.C.	No connection
6	-	N.C.	No connection
7	In	LINK_1CH	Number of channels linked in a secondary module *(internal pullup)* HIGH: One channel is linked LOW: Two channels are linked
8	-	5V	+5V supply
9	-	5V	+5V supply
10	-	N.C.	No connection
11	-	N.C.	No connection
12	In	PGM0	Bit 0 (lsb) of program number *(internal pulldown)*
13	In	PGM1	Bit 1 of program number *(internal pulldown)*
14	In	PGM2	Bit 2 of program number *(internal pulldown)*
15	In	PGM3	Bit 3 (msb) of program number *(internal pulldown)*
16	Out	REF_3V3	+3.3V output reference (10mA max)
17	In	VC_DELAY_4	Set delay time within the global time scale
18	In	VC_DELAY_3	Set delay time within the global time scale
19	In	VC_DELAY_2	Set delay time within the global time scale
20	In	VC_DELAY_1	Set delay time within the global time scale
21	In	CV_SCALE_MAX	Global scalar for maximum delay time
22	In	CV_SCALE_MIN	Global scalar for minimum delay time

<table>
<tr><th>Pin</th><th>I/O</th><th>Symbol</th><th>Description</th></tr>
<tr><td>23</td><td>-</td><td>GND</td><td>Ground</td></tr>
<tr><td>24</td><td>-</td><td>GND</td><td>Ground</td></tr>
<tr><td>25</td><td>In</td><td>SMP_RATE0</td><td rowspan="2">Sampling rate (internal pullup)
<table>
<tr><th>SMP_RATE1</th><th>SMP_RATE0</th><th>Sampling Rate</th></tr>
<tr><td>0</td><td>0</td><td>12kHz</td></tr>
<tr><td>0</td><td>1</td><td>24kHz</td></tr>
<tr><td>1</td><td>0</td><td>32kHz</td></tr>
<tr><td>1</td><td>1</td><td>48kHz</td></tr>
</table></td></tr>
<tr><td>26</td><td>In</td><td>SMP_RATE1</td></tr>
<tr><td>27</td><td>-</td><td>N.C.</td><td>No connection</td></tr>
<tr><td>28</td><td>Out</td><td>CLIPPING</td><td>Clipping indicator, 5mA max</td></tr>
<tr><td>29</td><td>In</td><td>OPTION_5</td><td rowspan="5">Digital control inputs (usage depends on the selected program). These inputs have an internal pullup and register as HIGH when disconnected.</td></tr>
<tr><td>30</td><td>In</td><td>OPTION_4</td></tr>
<tr><td>31</td><td>In</td><td>OPTION_3</td></tr>
<tr><td>32</td><td>In</td><td>OPTION_2</td></tr>
<tr><td>33</td><td>In</td><td>OPTION_1</td></tr>
<tr><td>34</td><td>In</td><td>TT_IN</td><td>Tap tempo, usage is program dependent</td></tr>
<tr><td>35</td><td>In</td><td>PRIMARY</td><td>Primary/secondary selector for multi-module systems. Module is PRIMARY when held high or not connected. (internal pullup)</td></tr>
<tr><td>36</td><td>Out</td><td>LINK_OUT</td><td>N.C on single modules or the last module in a multi-module configuration. Connected to downstream module’s LINK_IN in multi-module configurations.</td></tr>
<tr><td>37</td><td>In</td><td>LINK_IN</td><td>N.C. on single modules or the primary module in a multi-module configuration. Connected to the upstream module’s LINK_OUT in multi-module configurations.</td></tr>
<tr><td>38</td><td>In/Out</td><td>LINK_BUS_2</td><td>N.C. on single modules. Connected to all module’s LINK_BUS2 pins in multi-module configurations.</td></tr>
<tr><td>39</td><td>In/Out</td><td>LINK_BUS_1</td><td>N.C. on single modules. Connected to all module’s LINK_BUS1 pins in multi-module configurations.</td></tr>
<tr><td>40</td><td>-</td><td>N.C.</td><td>No connection</td></tr>
<tr><td>41</td><td>-</td><td>N.C.</td><td>No connection</td></tr>
<tr><td>42</td><td>-</td><td>N.C.</td><td>No connection</td></tr>
<tr><td>43</td><td>-</td><td>N.C.</td><td>No connection</td></tr>
<tr><td>44</td><td>-</td><td>N.C.</td><td>No connection</td></tr>
<tr><td>45</td><td>Out</td><td>AUDIO_OUT_4</td><td>Audio (tap) output 4</td></tr>
<tr><td>46</td><td>Out</td><td>AUDIO_OUT_3</td><td>Audio (tap) output 3</td></tr>
<tr><td>47</td><td>In</td><td>AUDIO_IN_3</td><td>Audio input 3</td></tr>
<tr><td>48</td><td>In</td><td>AUDIO_IN_4</td><td>Audio input 4</td></tr>
</table>

Notes:

N.C. pins must be left unconnected.

Unused audio and CV inputs should be tied to ground to minimize noise.

Unused outputs should be left unconnected.

Pinout Summary

Pin	Symbol		Pin	Symbol
1	AUDIO_IN_1		48	AUDIO_IN_4
2	AUDIO_IN_2		47	AUDIO_IN_3
3	AUDIO_OUT_1		46	AUDIO_OUT_3
4	AUDIO_OUT_2		45	AUDIO_OUT_4
5	N.C.		44	N.C.
6	N.C.		43	N.C.
7	LINK_1CH		42	N.C.
8	5V		41	N.C.
9	5V		40	N.C.
10	N.C.		39	LINK_BUS_1
11	N.C.		38	LINK_BUS_2
12	PGM0		37	LINK_IN
13	PGM1		36	LINK_OUT
14	PGM2		35	PRIMARY
15	PGM3		34	TT_IN
16	REF_3V3		33	OPTION_1
17	VC_DELAY_4		32	OPTION_2
18	VC_DELAY_3		31	OPTION_3
19	VC_DELAY_2		30	OPTION_4
20	VC_DELAY_1		29	OPTION_5
21	CV_SCALE_MAX		28	CLIPPING
22	CV_SCALE_MIN		27	N.C.
23	GND		26	SMP_RATE0
24	GND		25	SMP_RATE1

Specifications and Maximum Ratings

Item	Symbol	Range	Notes
Supply Voltage	5V	+4.5 to +5.5V	170mA
CV input voltage	CV_*	0 to REF_3V3	
Audio input	AUDIO_IN_*	0 to 2.6V p-p	AC coupled
Audio output	AUDIO_OUT_*	0 to 2.5V p-p	AC coupled
Audio input impedance		7-10kΩ	
Audio output load impedance		5kΩ	Min
Dynamic range		96dB	*(Theoretical, not yet measured)*
Signal-to-Noise ratio			*(Not yet measured)*

Program Selection

Configuration of the module is done by selecting a "program" using the 4 PGM pins. The program defines the basic topology of the delay lines (number of channels, number of taps, etc). Additional configuration options for some programs are done through the OPTION pins.

Upon power-up or a change in program selection, the white LED on the module will flash the program number (+1) to confirm operation of the module and the selected program. If an unused program number is selected, the LED will continuously fast-flash until a valid program is selected.

Summary of Programs

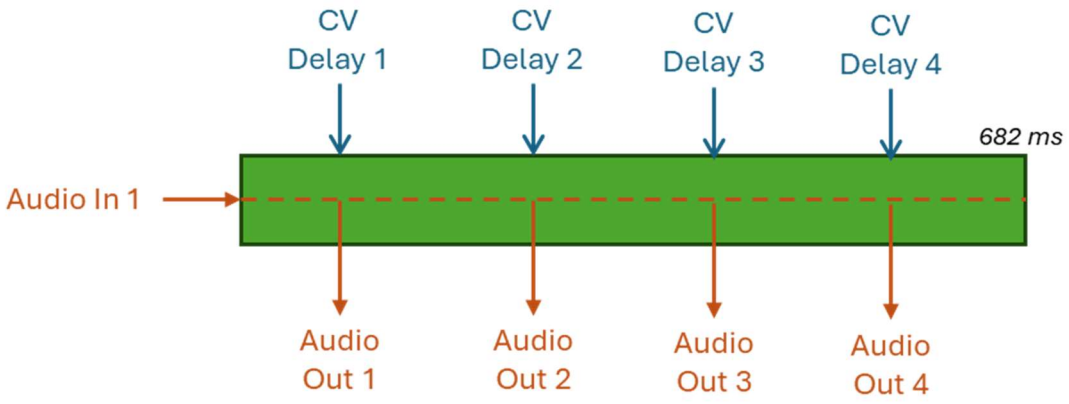
	Program 0 *(1) 682ms Delay*	**Program 1** *(2) 341ms Delays*	**Program 2** *(3) 227ms Delays*	**Program 3** *(4) 172ms Delays*
Channels	1	2	3	4
Taps/Channel	4	2	1 (+1 on chan 3)	1
Max Delay Time/Ch	682ms	341ms	227ms	170ms
Aliasing Support	Yes	Yes	Yes	No
AUDIO_IN_1	Chan 1 input	Chan 1 input	Chan 1 input	Chan 1 input
AUDIO_IN_2	Unused	Chan 2 input	Chan 2 input	Chan 2 input
AUDIO_IN_3	Unused	Unused	Chan 3 input	Chan 3 input
AUDIO_IN_4	Unused	Unused	Unused	Chan 4 input
AUDIO_OUT_1	Chan 1 tap 1	Chan 1 tap 1	Chan 1 tap 1	Chan 1 tap 1
AUDIO_OUT_2	Chan 1 tap 2	Chan 1 tap 2	Chan 2 tap 1	Chan 2 tap 1
AUDIO_OUT_3	Chan 1 tap 3	Chan 2 tap 1	Chan 3 tap 1	Chan 3 tap 1
AUDIO_OUT_4	Chan 1 tap 4	Chan 2 tap 2	Chan 3 tap 2	Chan 4 tap 1
CV_SCALE_MIN	Global scalar minimum delay			
CV_SCALE_MAX	Global scalar maximum delay			
CV_DELAY_1	Chan 1 tap 1 delay	Chan 1 tap 1 delay	Chan 1 tap 1 delay	Chan 1 tap 1 delay
CV_DELAY_2	Chan 1 tap 2 delay	Chan 1 tap 2 delay	Chan 2 tap 1 delay	Chan 2 tap 1 delay
CV_DELAY_3	Chan 1 tap 3 delay	Chan 2 tap 1 delay	Chan 3 tap 1 delay	Chan 3 tap 1 delay
CV_DELAY_4	Chan 1 tap 4 delay	Chan 2 tap 2 delay	Chan 3 tap 2 delay	Chan 4 tap 1 delay

	Program 4 *3 Delays + Stereo Eff*	**Program 5** *MN3011 Emulation*	**Program 6** *BBD Emulation*
Channels	3	1	4
Taps/Channel	1	6 (2 CT3280 reqd)	1
Max Delay Time/Ch	326ms chan 1 & 2	682ms	Varies by options
Aliasing Support	No	Yes	Yes
AUDIO_IN_1	Chan 1 input	Delay input	Chan 1 input
AUDIO_IN_2	Chan 2 input	Unused	Chan 2 input
AUDIO_IN_3	Chan 3 input	Unused	Chan 3 input
AUDIO_IN_4	Unused	Unused	Chan 4 input
AUDIO_OUT_1	Chan 1 tap 1	Fixed delay 4 / 6	Chan 1 output
AUDIO_OUT_2	Chan 2 tap 1	Fixed delay 3 / 5	Chan 2 output
AUDIO_OUT_3	Chan 3 LEFT	Fixed delay 2	Chan 3 output
AUDIO_OUT_4	Chan 3 RIGHT	Fixed delay 1	Chan 4 output
CV_SCALE_MIN	Global min delay		Unused
CV_SCALE_MAX	Global max delay		Unused
CV_DELAY_1	Chan 1 tap 1 delay	Unused	Chan 1 delay
CV_DELAY_2	Chan 2 tap 1 delay	Unused	Chan 2 delay
CV_DELAY_3	Unused	Unused	Chan 3 delay
CV_DELAY_4	Stereo field control	Unused	Chan 4 delay

The following sections describe each program and how they define the channels, delay times, and various options.

Program 0 (1 Delay, 4 Taps)

This program provides a single delay line with a maximum delay time of 682ms.

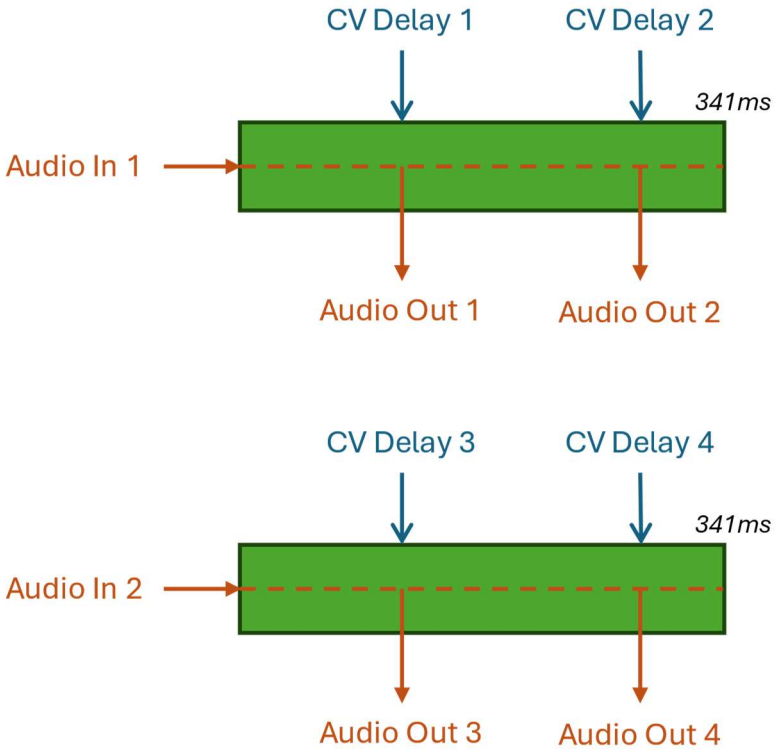


AUDIO_IN_1 is the delay line input, all other audio inputs are unused. Four delay outputs are available, each delay time independently controlled with the corresponding CV_DELAY value. The global MIN/MAX scalars apply to all taps. Note there is no required ordering of the delay taps, e.g. delay 1 could be longer than delay 3. All the taps are independently controlled by their corresponding CV delay input.

This program supports aliasing (see *Aliasing Feature* on page 17). Only the manual aliasing mode is supported. When aliasing is enabled, CV_DELAY_4 controls both the delay of output 4 and the intensity of the aliasing effect on all audio outputs.

Program 1 (2 Delay, 2 Taps)

This program is 2 delay channels with 2 taps each. Each channel has a maximum delay time of 341ms.

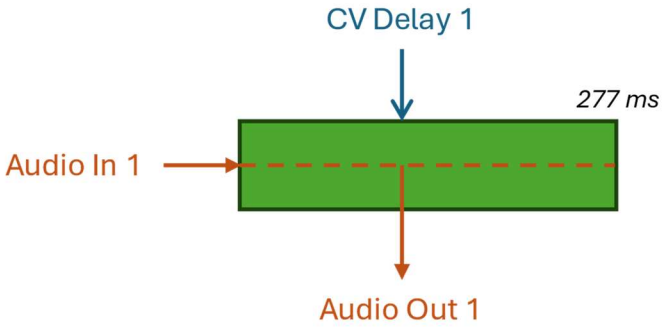


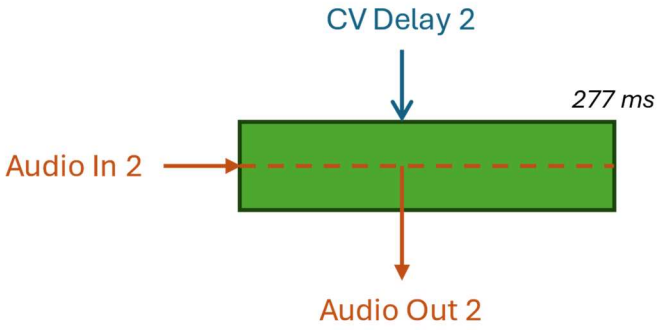
AUDIO_INPUT_1 and AUDIO_INPUT_2 are the inputs to the 2 channels, all other audio inputs are unused. Channel 1 has two taps provided at AUDIO_OUT_1 and AUDIO_OUT_2. Channel 2's outputs are AUDIO_OUT_3 and AUDIO_OUT_4. All taps for all channels are bounded by the global MIN/MAX scalars.

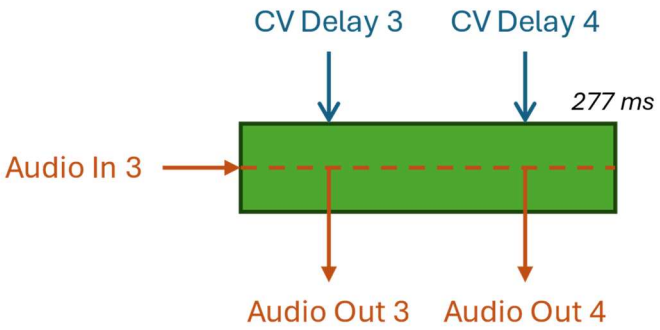
This program supports aliasing (see *Aliasing Feature* on page 17). Only the manual aliasing mode is supported. When aliasing is enabled, CV_DELAY_4 controls both the delay of output 4 and the intensity of the aliasing effect on all audio outputs.

Program 2 (2 Delays with 1 Tap, plus 1 Delay with 2 Taps)

This program provides 3 delay channels.





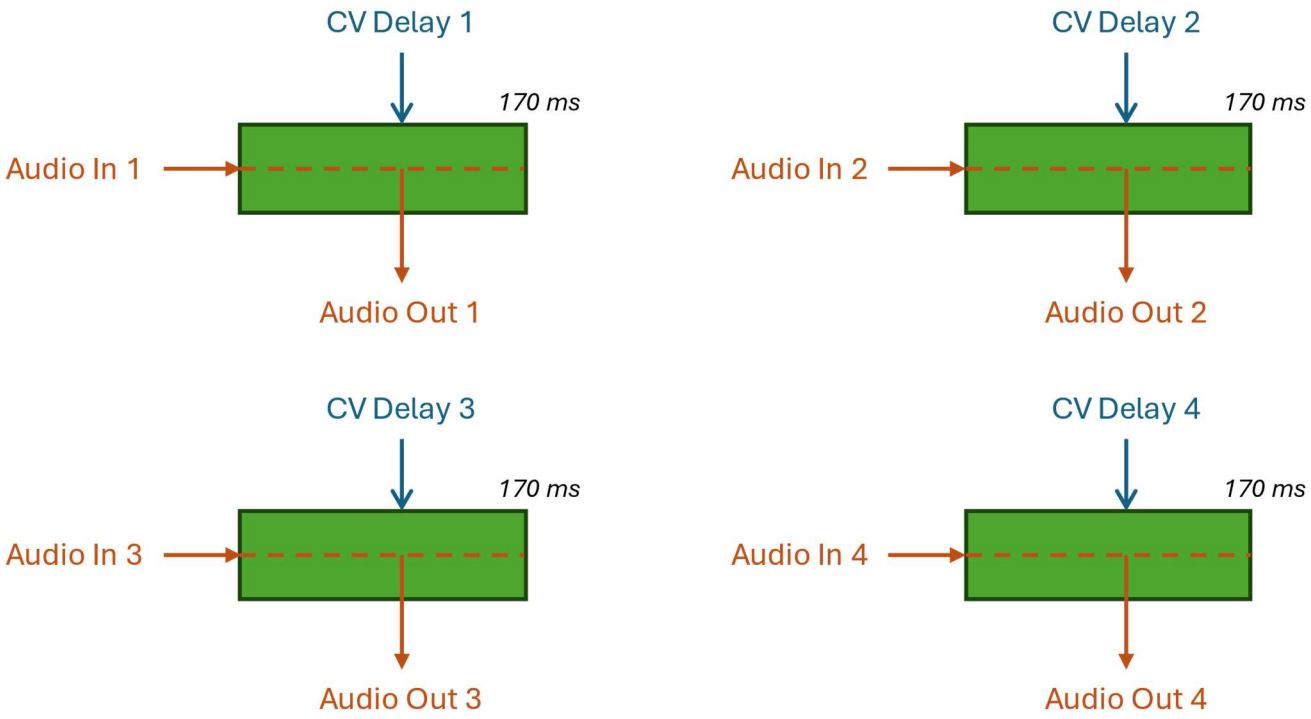


The first 2 channels (AUDIO_INPUT_1/2) have a single delayed output each (AUDIO_OUT_1/2). The third channel has 2 delayed outputs (ADUIO_OUT_3/4) controlled by CV_DELAY_3 and CV_DELAY_4. Maximum delay time for each channel is 277ms. The global MIN/MAX scalars apply to all delay times.

This program supports aliasing (see *Aliasing Feature* on page 17). Only the manual aliasing mode is supported. When aliasing is enabled, CV_DELAY_4 controls both the delay of output 4 and the intensity of the aliasing effect on all audio outputs.

Program 3 (4 Delays with 1 Tap each).

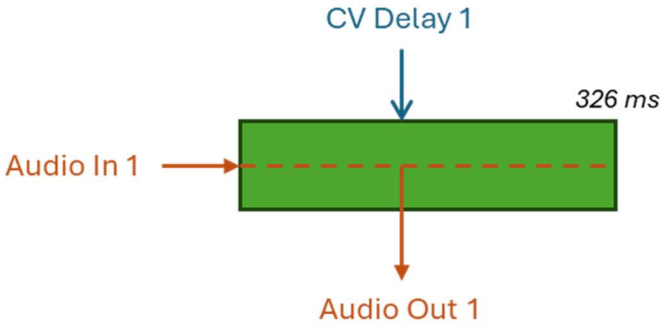
This program provides 4 delay channels each with a maximum delay time of 170ms.

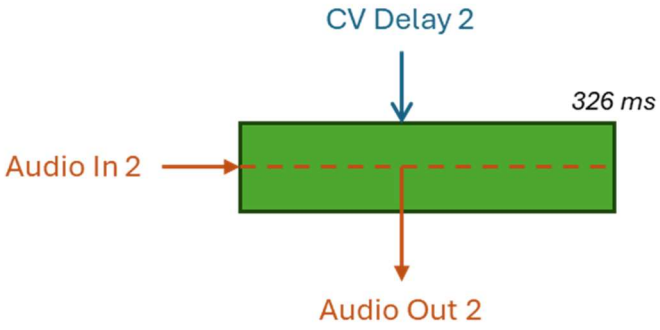


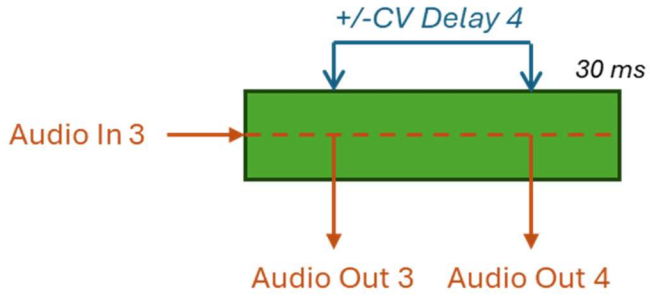
Each channel has a single delayed output controlled by the corresponding CV_DELAY_x value. The global MIN/MAX scalars apply to all delay times. This program does not support aliasing.

Program 4 (2 Delays with 1 Tap, plus a stereo effect pair output)

This is similar to Program 2 having 3 delay channels. The first two channels have a single delayed output, channel 3 outputs a variable stereo (Haas effect) on outputs 3 and 4.







The 3rd channel has no delay but produces a Haas stereo effect output with audio outputs 3 and 4 providing the L/R stereo pair. CV_DELAY_4 is used as the effect control. When the effect control is in the center of the range (1.65v) there is no stereo effect, both output channels will have the minimum (0.3ms) delay, e.g. the outputs are mono. When the control is < 1.65v delay is added to output 4 effectively moving the stereo field left. When the control is > 1.65v delay is added to output 3 moving the stereo field right. The amount of delay added is proportional to how far the effect control voltage is from center (1.65v). The maximum added delay is 30ms (at 0v left, and 3.3v right). The global MIN and MAX scalars have no effect on outputs 3 and 4.

This program does not support the aliasing feature.

Program 5 (MN3011 Emulation, two CT3280 modules recommended)

This program emulates the 6-tap delay structure of the MN3011 BBD delay chip. To use the full 6-tap capability of this program requires two CT3280 modules chained together (see *Chaining Multiple Modules* on page 19). If only a single module is used, this program will produce the first 4 taps of the MN3011. See the *MN3011 Emulation* section on page 14 for more details of this program and required hardware configuration.

This program supports aliasing (see *Aliasing Feature* on page 17). Only the manual aliasing mode is supported. To have consistent aliasing effects on all outputs, both modules of a 2-module configuration should have aliasing enabled and their VC_DELAY_4 lines should be tied together so the same aliasing intensity is used on all audio outputs.

Program 6 (General BBD Emulation)

This program provides emulation of many different BBD chips including all MN30XX models MN3001-MN3010 (see Program 5 for MN3011), plus SAD512/SAD1024, TDA1022, and V3205, V3207, V3208. This program provides 4 independent delay lines, one for each audio input/output pair. Each line will emulate one of the BBD chips based on the configuration selected. See *Configuration Selection* below.

Emulation consists of setting fixed minimum and maximum delay times based on the BBD datasheets. Since the min/max delay time is defined by the BBD model, the global VC_DELAY_MIN and VC_DELAY_MAX values are not used. Each of the four VC_DELAY_X inputs defines the delay of a particular channel within the range defined by the BBD model. For example, a delay line configured for an MN3009 will have a minimum delay of 0.64ms (VC_DELAY_X at 0.0V) and maximum of 12.8ms (VC_DELAY_X at 3.3V).

Configuration Selection

Configurations define which BBD chips are emulated on which delay channel. 4 BBDs can be emulated at a time, in combinations defined by the configuration.

1 of 8 configurations can be chosen by the OPTION_1, OPTION_2, and OPTION_3 inputs. These form a binary number which selects one of the configurations (see table below). Each configuration emulates 4 BBD chips, each BBD on an independent delay line. For example, when configuration zero is selected (OPTION pins 1,2,3 = LOW) delay line 1 emulates an MN3003, line 2 is an MN3006, line 3 is an MN3007, and line 4 is an MN3008.

Configurations 0 through 4 define various combinations designed to provide a wide variety of delay lines in each configuration. All BBD models are represented in at least one of the configurations. Configurations 5 through 7 provide dual delay lines of 2 selected types useful for stereo applications.

The following table shows which BBDs (and associated delay times) are on which channels for each of the 8 configurations. To see which BBDs are in a particular configuration, read one column of the table. Min and max delay times are in msec.

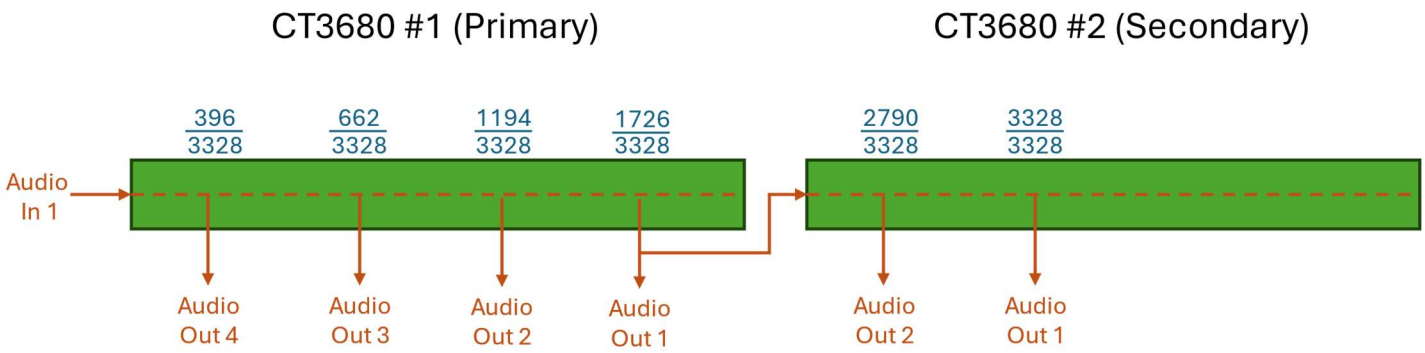
		Configuration selected by OPTION pins [3:2:1]							
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
LINE 1	*BBD*	MN3003 54.7%	MN3009 54.7%	MN3006 54.7%	MN3009 54.7%	MN3006 54.7%	MN3006 54.7%	MN3001 MN3002 89.6%	MN3009 54.7%
	Min	*0.16	0.64	0.32	0.64	0.32	0.32	0.32	0.64
	Max	3.20	12.80	6.40	12.80	6.40	6.40	25.60	12.80
LINE 2	*BBD*	MN3006 54.7%	MN3001 MN3002 89.6%	MN3004 MN3010 4.4%	MN3007 4.4%	V3207 54.7%	MN3006 54.7%	MN3001 MN3002 89.6%	MN3009 54.7%
	Min	0.32	0.32	2.56	5.12	2.56	0.32	0.32	0.64
	Max	6.40	25.60	25.60	51.20	51.20	6.40	25.60	12.80
LINE 3	*BBD*	MN3007 4.4%	SAD512 SAD1024 93.6%	V3207 54.7%	MN3008 V3208 4.4%	MN3005 V3205 4.4%	MN3007 4.4%	MN3008 V3208 4.4%	MN3005 V3205 4.4%
	Min	5.12	*0.17	2.56	10.24	20.48	5.12	10.24	20.48
	Max	51.20	170.67	51.20	102.40	204.80	51.20	102.40	204.80
LINE 4	*BBD*	MN3008 V3208 4.4%	MN3005 V3205 4.4%	MN3008 V3208 4.4%	TDA1022 81.6	MN3005 V3205 4.4%	MN3007 4.4%	MN3008 V3208 4.4%	MN3005 V3205 4.4%
	Min	10.24	20.48	10.24	51.20	20.48	2.12	10.24	20.48
	Max	102.40	204.80	102.40	512.00	204.80	51.20	102.40	204.80

(*) BBDs with a min delay < 0.3ms will have an emulated min delay = 0.3ms (MN3003 and SAD512).

This program supports the *Aliasing Feature* as described on page 17. Aliasing is enabled by making the OPTION_5 input pin LOW. Aliasing is controlled by CV_DELAY_MIN (which is otherwise unused in this program). This program supports only ***manual mode*** aliasing whereby the intensity of the effect is determined by the CV_DELAY_MIN input. An input of 0.0V will produce no effect, and 3.0V produces the maximum effect.

MN3011 Emulation

Program #5 emulates the 6 fixed-tap delay structure of a MN3011 BBD chip. MN3011 emulation is achieved by fixing the CT3680 delay tap ratios to the delay intervals of the physical MN3011 BBD chip.

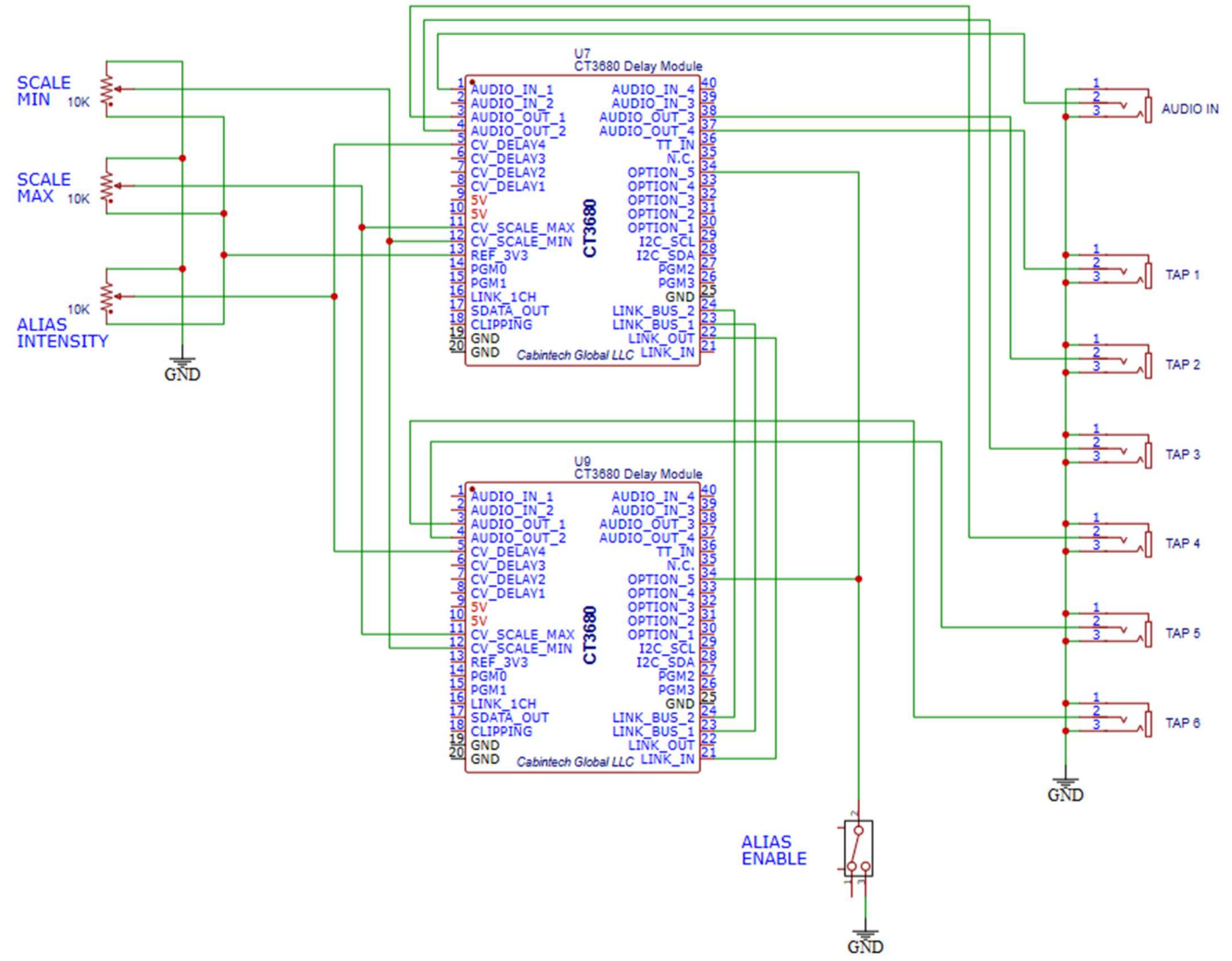


Those delay time ratios are scaled into the global MIN/MAX delay times as set by their respective CV values. When two modules are used for the 6-tap configuration, the MIN/MAX inputs of the two modules must be tied together (e.g. both modules get identical MIN/MAX CVs). This is in addition to the connections required for all module chaining configurations as described in the *Chaining Multiple Modules* section. If only a single module is used it will produce the first 4 tap intervals and no special hardware configuration is required.

If the aliasing feature is used with this program, the OPTION_5, and CV_DELAY_4 (alias intensity) of both modules should be tied together so that all outputs have consistent aliasing effects applied.

Since the delay intervals are fixed, the CV_DELAY_1/2/3 inputs of both modules are unused. All the output delays are determined by mapping the MN3011 intervals into the MIN/MAX global range. The first 4 taps are produced by the first (*primary*) module on AUDIO_OUT_4/3/2/1 (e.g. the shortest MN3011 tap is produced on AUDIO_OUT_4 of the first module, the 2nd shortest on AUDIO_OUT_3, the 3rd on AUDO_OUT_2, and the 4th tap is on AUDIO_OUT_1). The last 2 taps are produced by the second module on AUDIO_OUT_2/1 (5th tap on AUDIO_OUT_2 and the longest tap on

AUDIO_OUT_1). Audio outputs 3 and 4 of the second module are unused.



In the current implementation, it is possible to emulate MN3011 delay intervals over a wider range than the physical MN3011 supports. At its maximum and minimum clock speeds the MN3011 supports delay ranges of 2.0-16.6ms (100kHz clock) to 19.8-166.4ms (10kHz clock). The CT3280 supports delay ranges from 0.9-5.0ms to 81-682ms. The following table shows some typical MIN/MAX settings and the resulting delay times for each output. For reference, the MN3011 delay times at minimum and maximum clock rates are also shown.

MN3011 Delays (ms)		
	Clock (kHz)	
Outputs	100	10
1	2.0	19.8
2	3.3	33.1
3	6.0	59.7
4	8.6	86.3
5	14.0	139.5
6	16.6	166.4

CT3680 Program 5 Delays (ms)												
Module	Tap	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
		5	0.3	17	0.3	167	0.3	200.4	50.1	682	0.3
1	4	0.9		2.0		19.8		68.0		81.4	
	3	1.2		3.3		33.2		80.0		135.9	
	2	2.0		6.0		59.8		104.0		244.9	
	1	2.7		8.7		86.5		128.1		353.8	
2	2	4.2		14.0		139.8		176.1		571.8	
	1	5.0		16.7		166.7		200.4		682.0	

Aliasing Feature

Some programs of the CT3680 support an 'aliasing' feature that emulates the behavior of physical BBD devices when they are run at lower clock speeds (e.g. longer delay times). Aliasing is a form of distortion caused by sampling the audio at a rate lower than 2 times the maximum audio frequency. Since the CT3680 always samples at 48kHz it does not naturally induce aliasing in the audio band at any delay time. This feature simulates the aliasing effect of lower sampling rates.

The OPTION_5 pin enables aliasing mode when it is set LOW. By default (no connection on the OPTION_5 pin), the aliasing feature is disabled.

OPTION_5	Aliasing Effect
N.C.	Disabled
HIGH	Disabled
LO	Enabled

The intensity and mode of the aliasing effect can be controlled by one of the VC inputs (as defined by the selected program). In ***manual mode*** (VC range 0.0V to 3.0V), the intensity is set by the sweep of the VC input such that an input voltage of 0.0V will cause no effect (48kHz sampling) and an input voltage of 3.0V will simulate a sampling rate approaching zero. This CV input can be set to any level of desired aliasing, or it can be varied over time or in sync with the delay settings. The intensity level set by this CV input may be used for a subset or all of the audio outputs (see the individual program descriptions for how this effect is applied to outputs).

Some programs support ***automatic mode*** aliasing. When the aliasing CV input is set to full scale (or any value above 3.0V) the aliasing is set to automatic mode (for programs that support it). In automatic mode the intensity of the aliasing is automatically determined by the delay settings to simulate real BBD hardware in which the aliasing effect is more intense at longer delay times. See the individual program settings for how automatic aliasing intensity is determined. If the program does not support automatic aliasing, then the CV inputs above 3.0V have the same effect as 3.0V.

When manual aliasing is at its most extreme setting (3.0V) this can cause the audio to drop out because the output signal approaches DC (constant value).

If multiple modules are chained together, in general it is desirable that they all produce the same aliasing effect (although it is not required). To achieve that, the OPTION_5, and aliasing VC input of all modules in the chain should be tied together. See the *Chaining Multiple Modules* section on page 19.

Setting Delay Times

Delay CV Inputs

Delay times in the CT3680 are defined by CV (control voltage) inputs in the range of 0.0v to +3.3v. A minimal CV input (0.0V) indicates a minimum delay time, and a maximum CV input (+3.3V) indicates a maximum delay time. CV values between 0.0V and 3.3V define a linear scaling of delay time between the minimum and the maximum. What actual delay times those represent depends on the global delay scalars (see next section) and the currently selected program (see *Program Selection* on page 7). The CT3680 is capable of delay times from 0.3ms to 682ms. The maximum delay for any given channel depends on the selected program. Unused audio and CV inputs should be tied to ground to minimize noise. Unused outputs should be left unconnected.

Global Scalars

Two CV inputs (CV_SCALE_MIN, CV_SCALE_MAX) define a global range for all delay times. All individual tap delays on all channels are scaled to be in the range of MIN-MAX. This allows tap delay CV inputs to use their full scale (0.0V to 3.3V) to cover a range of delay values that are of use for a particular application. (It would be unusual for an effect to use delay times across the full device capability of 0.3 to 682ms). With a narrower global range, the CV tap inputs operate with more precision in the delay range of interest and makes them less susceptible to noise.

For example, if a module is to operate as a 2 channel delay with delay times between 100ms and 200ms, then program 1 would be selected since it defines a 2 channel configuration. The table in the *Program Selection* section shows the max capable delay time for that program is 341ms. To set a global minimum delay to 100ms, the CV_SCALE_MIN would be set to (100ms/341ms)*3.3v = 0.97v. To set a global maximum of 200ms, CV_SCALE_MAX would be set to (200ms/341ms)*3.3v = 1.94v.

With those global MIN/MAX settings, the CV inputs (CV_DELAY_x) used to set the individual tap delay times have a full scale range of 100ms to 200ms. E.g. setting CV_DELAY_1 to 0.0v would result in channel 1 tap 1 to be delayed 100ms (global MIN). Setting it to its halfway point (3.3/2=1.65v) would result in a delay time halfway between global MIN and MAX, e.g. 150ms. Setting it to full scale 3.3v results in a delay time of 200ms (global MAX).

The global MIN and MAX times apply to all channels and all taps. Note that the global MIN and MAX delay time CV inputs are really a differential pair. It is not required that VC_SCALE_MAX be greater than VC_SCALE_MIN. The lower of the two CVs defines the global minimum delay time and the higher of the two defines the global maximum delay time. If the values are the same, then all delays are constrained to that single value (or narrow range).

All CV inputs, including the global scalars, may be modulated (varied with time) to achieve various effects.

Chaining Multiple Modules

Overview

This feature allows multiple modules to be (digitally) chained to achieve longer delay times and/or more taps without signal degradation. The limit of how many modules can be chained depends on the integrity of the shared bus signals but 5 modules should be chainable with no additional hardware.

Chained modules are defined by a single ***Primary*** module (the PRIMARY input pin is HIGH) and some number of downstream ***Secondary*** modules (with the PRIMARY input pin pulled LOW). There can be only a single primary module in a linked system. LINK signals must be connected between the modules as described in this section. A primary module copies its AUDIO_OUTPUT_1 to the Secondary module's AUDIO_INPUT_1. This is a digital copy so

chaining multiple modules does not degrade the audio quality. The Primary module's analog output 1 is still active and can be used as a delay output as usual. The secondary's analog input 1 is not used. If desired, 2 channels can be linked by tying the LINK_1CH input pin low on the secondary module. When that pin is LOW, outputs 1 **and 2** of the Primary are copied to inputs 1 **and 2** of the secondary.

There are many possible uses for module chaining. In the simplest case, it can be used to achieve a longer overall delay time than the 682ms maximum of a single module. If, for example, a delay time of 750ms was desired (3/4 sec), the first module in the chain could implement a delay with Program 0 and set Tap 1 delay time to 500ms. Tap 1 output is copied to input 1 of the second module via the digital chain. If that module is also running Program 0, then it can add up to 682ms additional delay. By setting the MIN/MAX scalars and Tap delay CV signals appropriately, it could add 250ms delay to its Tap 1 output, thus achieving a 750ms delay from input 1 to the first module, to output 1 of the second.

Another use of chaining is to achieve more delay taps (analog audio outputs) than the 4 outputs supported by a single module. More outputs allow for a richer variety of delayed signals to mix, filter and process. Program 5 (MN3011 emulation) uses 2 modules to emulate the 6 taps of the MN3011 BBD chip.

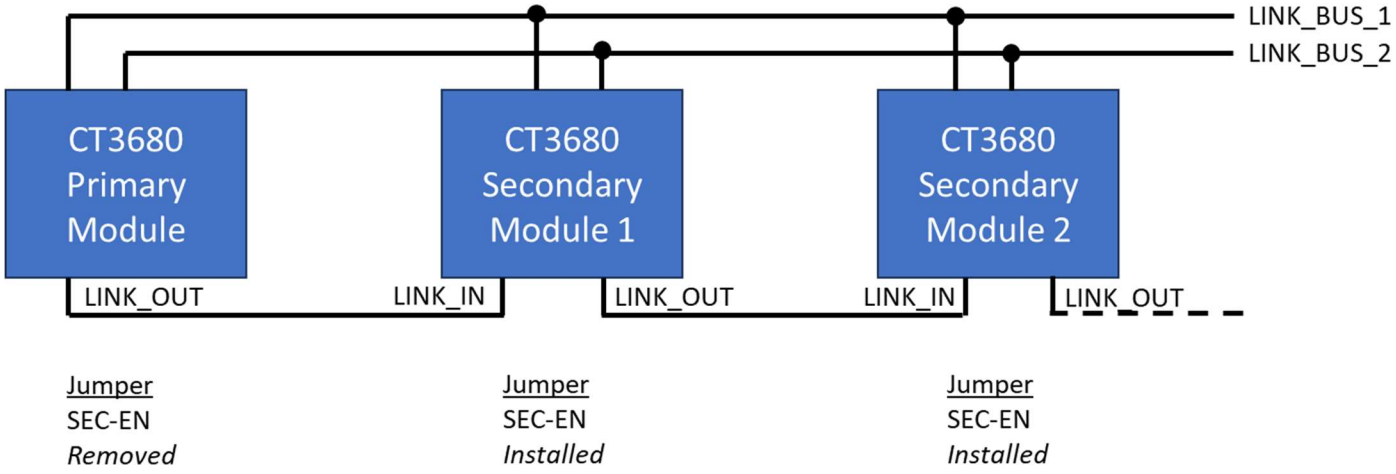
Cumulative Delay

Because downstream modules read their input 1 (and possibly input 2) from upstream (delayed) outputs, delay is cumulative from module to module down the chain. Note that each module is always limited (by program selection) in the total amount of delay it can add, and that if a module changes the delay of Tap 1, that change propagates to all downstream modules. Since each module can be running a different Program, a wide variety in number of delay channels and total delay times can be achieved. Chaining is always limited to passing 1 or 2 audio outputs from one module to the next.

Tap 1 (AUDIO_OUT_1) of the upstream modules is copied to input 1 of the downstream module (and possibly out 2 to input 2), but all the analog outputs of the upstream module (including analog outputs 1 and 2) are active and behave according to the selected program. Also note that if a downstream program defines multiple delay channels, only the channel driven from input 1 (and possibly 2) receives data from the upstream module; all other channels of the downstream module run independently within that module and may process completely independent audio signals.

Hardware Configuration

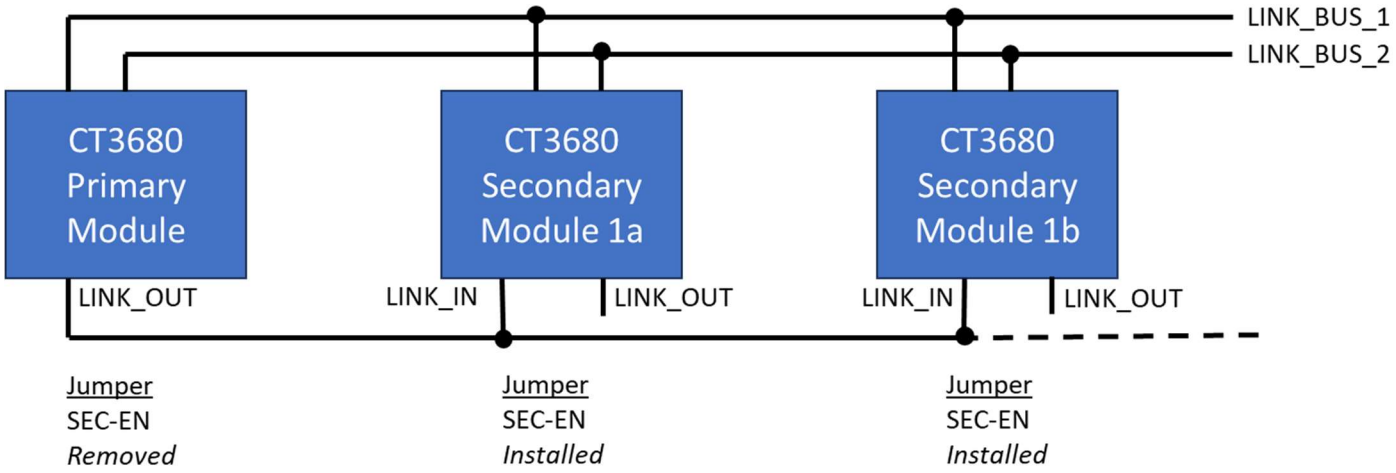
To achieve chaining, one module is designated as the ***Primary*** module, all others are ***Secondary*** modules. All modules in the chain must be connected together by their LINK_BUS_1 and LINK_BUS_2 pins. On each upstream/downstream pair, the upstream LINK_OUT must be connected to the downstream LINK_IN. These are digital signal lines so PCB layout should be done accordingly. All modules should share a common ground and power supply.



When modules are chained together, the PRIMARY module pin is held HIGH (or unconnected), all others (the *Secondary* modules) must have the PRIMARY pin held LOW.

All secondary modules in a chain have the analog AUDIO_IN_1 disabled, and audio is instead copied (digitally) from AUDIO_OUT_1 of the nearest upstream module. Depending on the program selected in the downstream module, other analog audio inputs may be active. Module audio chaining is always AUDIO_OUT_1 of the upstream module to AUDIO_IN_1 of the downstream module (and AUDIO_OUT_2 to AUDIO_IN_2 when 2-channel linking is enabled via the LINK_1CH input pin). AUDIO_OUT_1 and AUDIO_OUT_2 may also be used as a normal analog outputs on any of the modules of the chain.

It is also possible for a Primary (or any upstream) module to drive multiple downstream modules, copying its output(s) to the input(s) of more than one downstream module. In this example, the Primary module output 1 is digitally copied to the input 1 of both modules 1a and 1b.



The topology can mix single and multiple downstream modules in a system, but there can be only 1 Primary module, and no more than 5 total.

Chained Programs

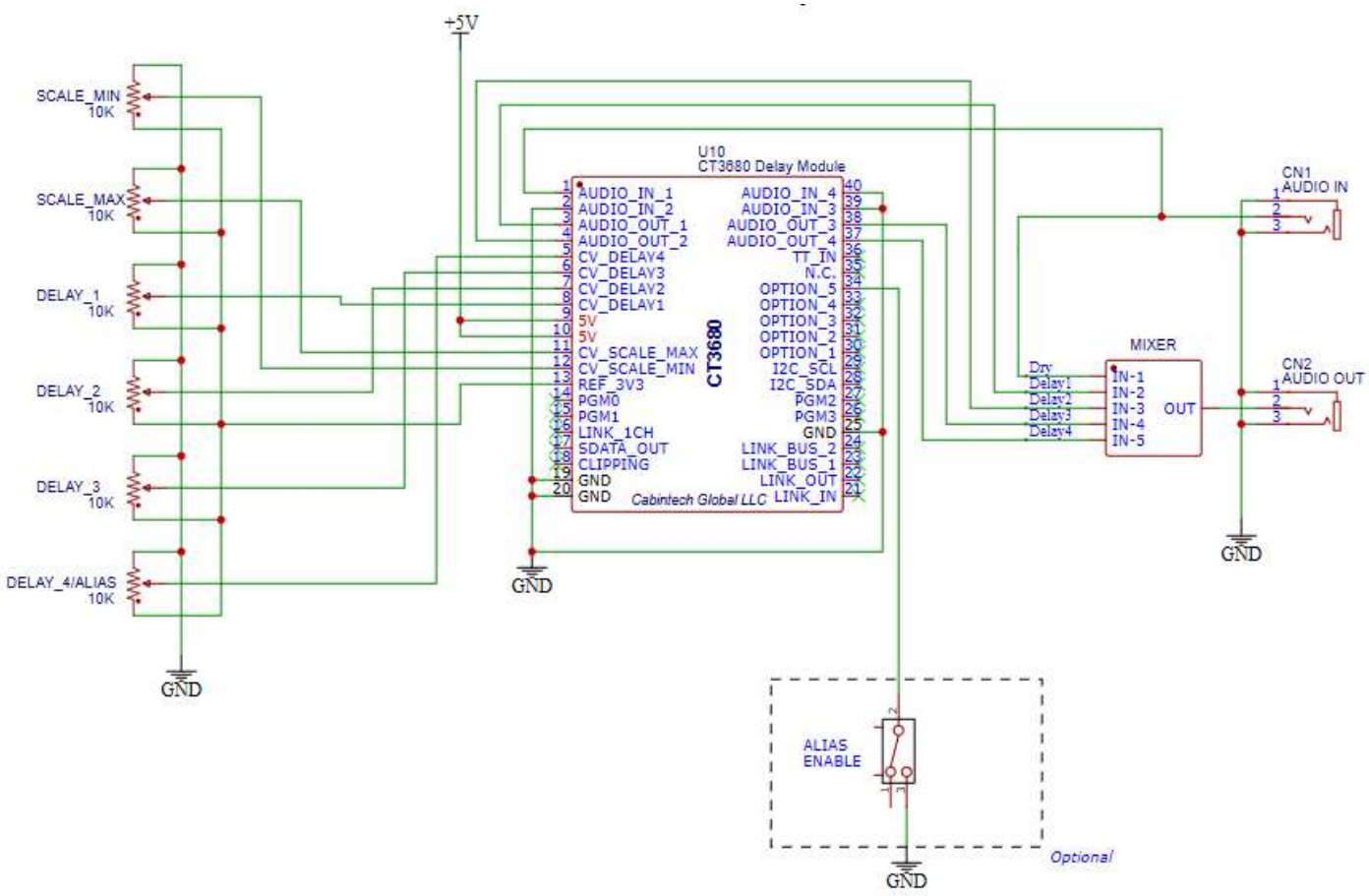
Each module in the chain selects its program setting with its own set of PGM input pins (see *Program Selection* on page 7). It is not required that every module run the same program but note that AUDIO_INPUT_1/2 is disabled on all downstream modules, programs that read input 1 will instead read output 1 of the upstream module as their input. Some programs are designed for multi-modules configurations (e.g. Program 5, the MN3011 emulation program) in which case that program should be selected on all the modules.

In general, it is not required that global MIN/MAX scalars be linked between modules in any particular way. Modules in the chain may each have their own independent scalars, or a single CV can be used to drive the MIN/MAX on multiple modules. Other inputs may or may not be tied together depending on the application.

Typical Applications

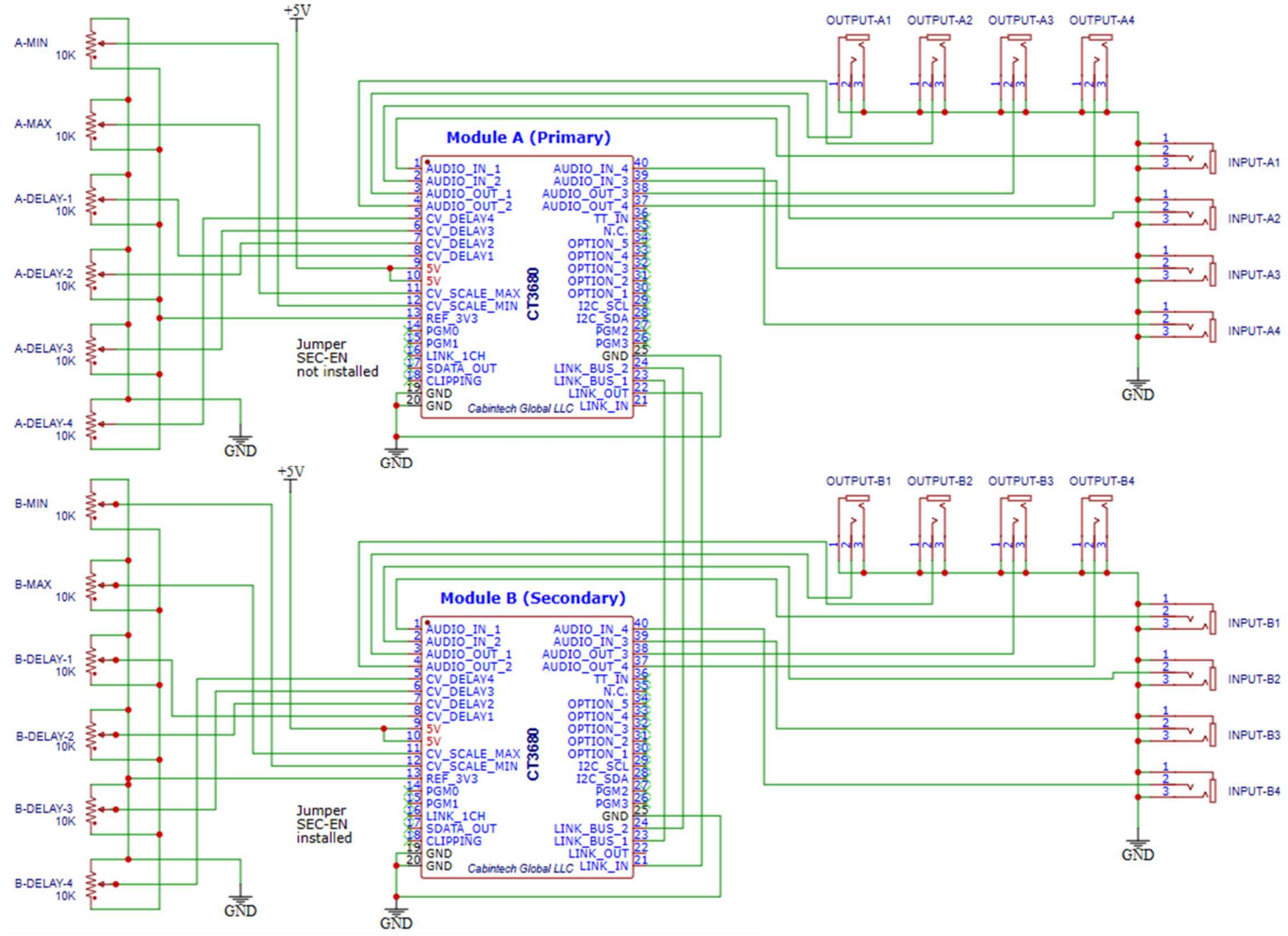
Minimum Reference Schematic

This represents a minimum circuit to implement a 1 line, 4 tap delay with manual (potentiometer) CV controls. For this configuration the program jumpers would be set to program 0 (all PGM pins held LOW). The mixer here is conceptual, to show that the original (dry) signal and the various delayed signals might be mixed at various relative levels to produce a single audio output.



Primary/Secondary Linked Modules

This is a minimum circuit to implement an 8 input, 8 output delay system composed of two linked CT3680 modules with manual CV controls. Both modules should share a common ground and power supply. They may also have shared inputs such as the alias feature controls (OPTION_5, and a CV_DELAY input), depending on the application.



Physical Dimensions, Mounting, and Adapters

Board outline 0.0mm x 0.00mm.

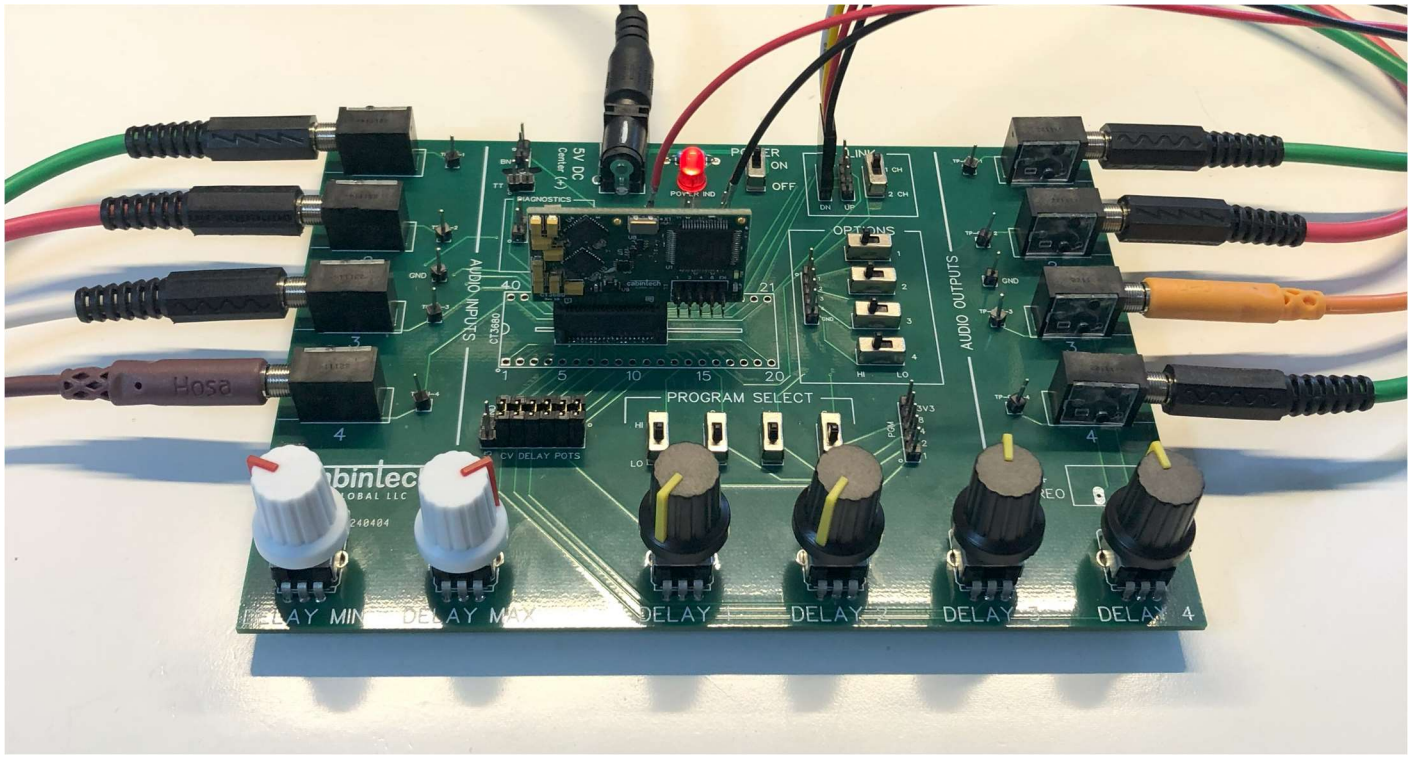
PCB Design Notes

When designing a PCB on which the CT3680 will be used, note the following guidelines:

1. Adjacent +5 and GND pins should both be connected to the appropriate PCB traces. When possible, use larger track sizes for power and ground connections.
2. Any pin noted as "N.C." in the *Pinout* section on page 3 should be left unconnected on the PCB. Do not tie these pins to power or ground.
3. Schematic symbols, PCB footprints, 3D models, and other design resources are available on the Cabintech website. Symbols and footprints can help avoid errors in the schematic connections and PCB layout.

Development / Breakout Board

A development board is available to aid in prototyping and development of CT3680 based products. The dev board makes all the inputs and outputs of the module accessible through header pins and connectors. The board has 6 potentiometers for manual CV control and switches for setting the program number and option inputs. Audio inputs and outputs are available through standard TS (mono) 3.5mm jacks, as well as a TRS (stereo) connector that combines audio outputs 3 and 4. The dev board also has probe points for all pins of the module as well as headers for signals that may be processed off-board.



Development Board Features

- 6 potentiometers for CV controls
- 4 program select switches
- 5 option select switches
- Power connector jack
- Power on/off switch and LED
- 8 mono (TS) 3.5mm audio input/output jacks
- 1 stereo (TRS) 2.5mm audio output jack (combines outputs 3+4 into L+R)
- Header pins for all audio inputs and outputs
- 5V, 3.3V, and GND header pins
- Headers for upstream and downstream linked modules
- Switch for 1 or 2 channel linking
- Test points for all pins of the CT3680 module

Power Supply

The power section of the dev board has a 2.1mm power jack (*center positive*) for +5V power input, an ON/OFF switch, and a LED. The ON/OFF switch allows control of power to the module without removing and inserting the power plug. The power indicator LED lights when the module is powered (as a reminder not to insert or remove the module while the power is ON). Double header pins are supplied for off-board access to 5V, 3.3V, and GND. When using multiple development boards it is handy to jumper the 5V supply and GND lines together so only one board needs to have a power plug. *Do not tie 3.3V supplies of multiple boards together. Each board generates its own independent 3.3V supply via a regulator on the module.*

Program Selection

The board has 4 program selection switches to allow setting the program via the module's PGM pins. The program select lines are also made available on header pins so program selection can be controlled off-board (for example, by a microcontroller*). When driving the program select lines off-board, the switches must remain in the LOW (off) position.*

Option Selection

The board has 5 selection switches in the OPTIONS section that allow control of various program options. Header pins make option control available to an off-board controller. *When driving the option pins off-board, the option switches must remain in the HI position.*

Delay (CV) Controls

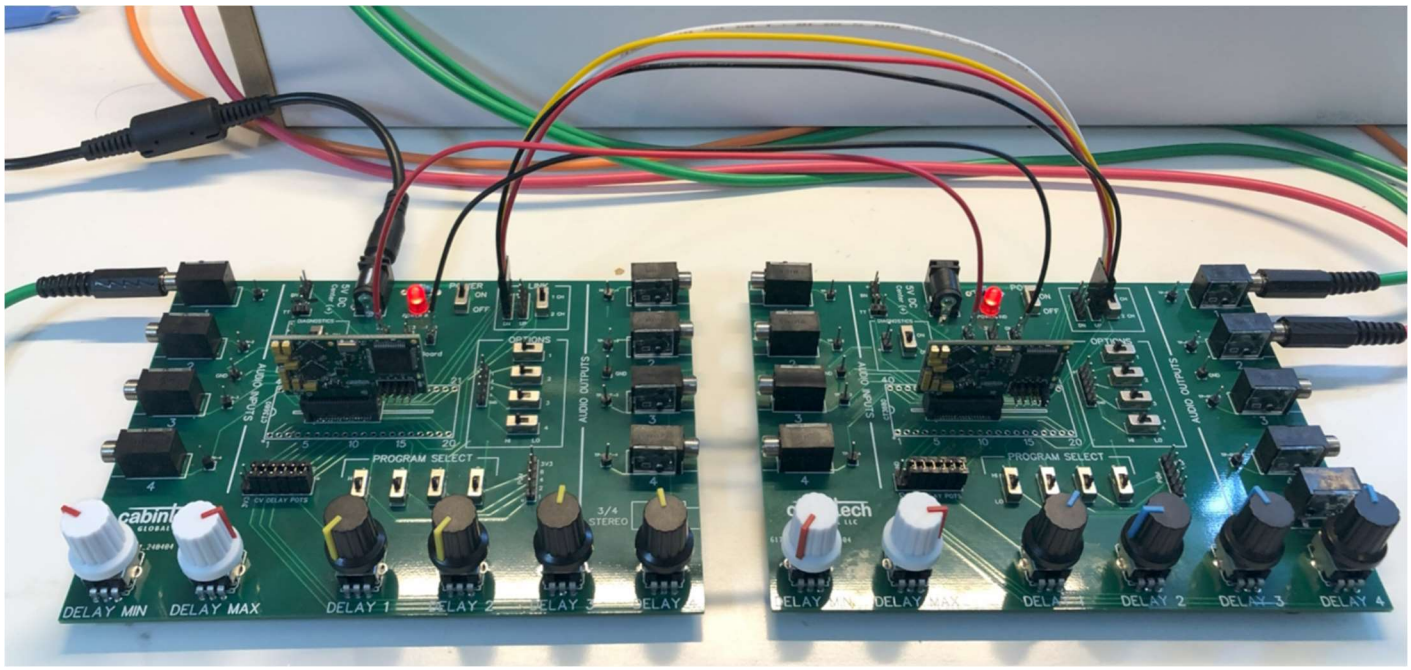
The board has 6 potentiometers along the bottom edge for control of the min/max/1/2/3/4 delay parameters. At the full counterclockwise position, the CV voltage will be 0.0V, full clockwise is 3.3V. The potentiometers are linear. If CV is to be supplied off-board, the CV control jumpers should be removed, and the external CV signals should be supplied to the upper pins of the jumper block (closest to the CT3680 module). *When driving the CV controls from off-board, the CV jumpers must be removed.* The jumper block also contains GND and 3.3V pins for off-board reference. *Be sure not to install a jumper across the GND/3.3V pins.*

Audio Input/Output

3.5mm TS mono jacks are provided for the (4) audio input and (4) audio outputs of the CT3680 module. Each input and output also have a single header pin that is handy for clipping test leads to. There is also a single TRS stereo output jack that combines audio outputs 3/4 into a left/right stereo pair.

Multi-Module Linking

The board has two headers in the LINK section for linking modules as described in *Chaining Multiple Modules* on page 19. Each header has 4 pins. The *primary* module development board should have its "DN" (downstream) header connected to the *secondary* module board's "UP" (upstream) header. Connect all 4 pins of the header from one board to the next. If a secondary board is to be connected to another secondary board, connect its DN header to the next board's UP header, and so on, down the chain of boards.



Linked development boards

For secondary module boards, the switch in the LINK section can be set to “1 CH” for single channel linking, or “2 CH” for dual channel linking.

Revisions

Rev	Date	Changes
Rev 1	April 29, 2024	First public release
Rev 2	May 9, 2024	Added Program 6 description (General BBD Emulation)
Rev 3	May 13, 2024	Updated development board details
Rev 4	July 10, 2024	Revised for V1.1 of the hardware

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