Dual Voltage Controlled Amplifier

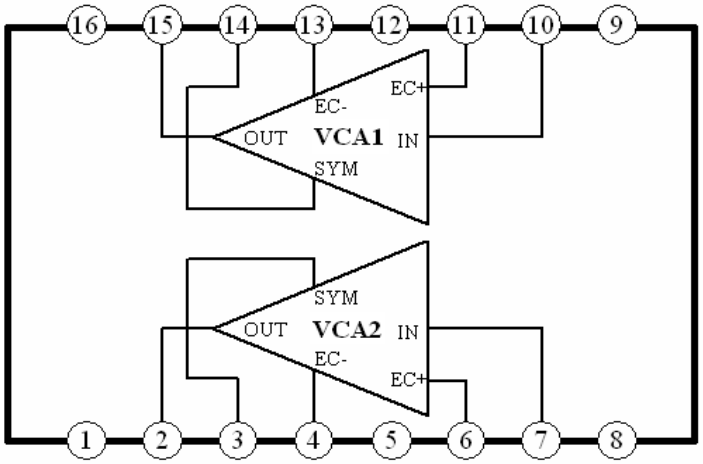
1、Overview

The V2162 is a dual voltage-controlled amplifier (VCA) that designed for typical applications such as audio compressors/limiters, equalizers and oscillators. The chip is a high-performance current-in/current-out device with two opposing-polarity, voltage-sensitive control ports in each channel. Fabricated in a low-noise process utilizing high h_{FE}, complementary NPN/PNP pairs, the V2162 can offer high performance with minimal support circuitry. Its features are:

- Two Independent VCA Channels
- Wide Dynamic Range: >115dB
- Wide Gain Range: >130dB
- Exponential (dB) Gain Control
- Low Distortion: 0.04% typ.
- Dual Control Ports (pos/neg)
- Package: SOP16L

2、Block Diagram and Pin Description

2. 1、Block Diagram



2. 2、Pin Description and Structure Scheme

Pin	Symbol	Function	Pin	Symbol	Function
1	NC	No connection	9	NC	No connection
2	OUT1	Signal output 1	10	IN2	Signal input 2
3	SYM1	Symmetry control input 1	11	EC+2	Gain control input 2 positive
4	EC-1	Gain control input 1 negative	12	V_{CC}	Positive power supply
5	V_{EE}	Negative power supply	13	EC-2	Gain control input 2 negative
6	EC+1	Gain control input 1 positive	14	SYM2	Symmetry control input 2
7	IN1	Signal input 1	15	OUT2	Signal output 2
8	GND	Ground	16	NC	No connection

3、Electrical Characteristics

3. 1、Absolute Maximum Ratings

Unless otherwise specified，T_{amb}= 25℃

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}/V_{EE}	±18	V
Operating Temperature	T_{OP}	-20~75	℃
Storage Temperature	T_{stg}	-40~125	℃
ESD Tolerance(HBM)	V_{ESD}	2	kV

3. 2、Recommended Operating Conditions

Parameter	Symbol	Condition	Limit			Unit
			Min	Typ	Max	
Supply Voltage	V_{CC}/V_{EE}		±4	±15	±16	V
Signal Current	$I_{IN}+I_{OUT}$	Supply Voltage: ±15V		125	550	μA

3. 3、Electrical Characteristics

(Unless otherwise specified, T_{amb} =25℃,V_{CC}=+15V, V_{EE}=-15V)

Parameter	Symbol	Test Conditions		Value			Unit
				Min	Typ	Max	
Supply Current	Icc	No Signal			4.8	6	mA
Equivalent Input Bias Current	I_B	0dB Gain			5	20	nA
Input Offset Voltage	$V_{OFF(IN)}$	0dB Gain			10		mV
Output Offset Voltage	$V_{OFF(OUT)}$	R_{OUT}=20kΩ,0dB gain, THD adj for min			±1		mV
Gain Cell Idling Current	I_{IDLE}	0dB Gain			20		μA
Max. I/O Signal Current	$I_{IN(VCA)}$+ $I_{OUT(VCA)}$	0dB Gain			±1.4		mA_{peak}
Gain-Control Constant	E_C/Gain（dB）	-60dB<Gain<40dB	EC+	5.8	6.0	6.2	mV/dB
			EC-	-5.8	-6.0	-6.2	
Gain-Control Temp. Co	△EC/△T_{CHIP}	Ref. T_{CHIP}=27℃			0.33		%/℃
Gain-Control Linearity		-60~40dB Gain			1		%
Off Isolation		E_C+=-0.36V,Ec-=+0.36V		110	115		dB
Output Noise	$e_{N(OUT)}$	20Hz~20kHz, R_{OUT}=20kΩ	0dB		-97	-89	dBV
			15dB		-88	-82	
Symmetry Control Voltage	V_{SYM}	0dB Gain, THD<0.07%		-4	0	4	mV
Total Harmonic Distortion	THD	I_{OUT}=30μA 1kHz	0dB		0.04	0.07	%
			20dB		0.075	0.10	
			-20dB		0.075	0.15	

4、Test Circuit

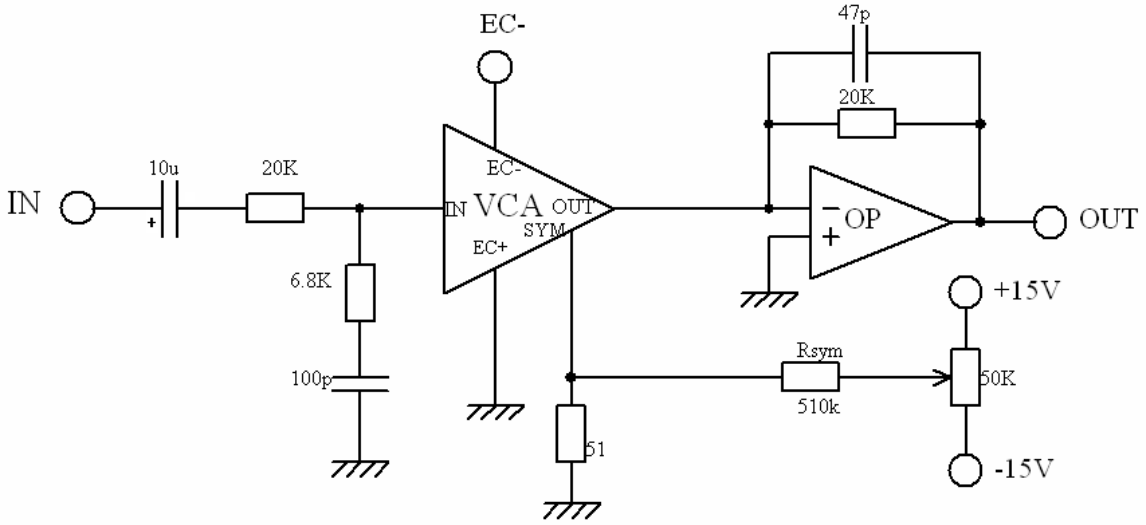


Figure 1. Test Circuit (Single Channel)

5、Characteristics Curve

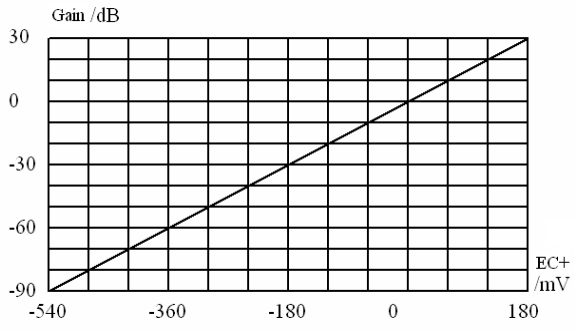


Figure 2. Gain Vs. Control Voltage (EC+) @ 25℃

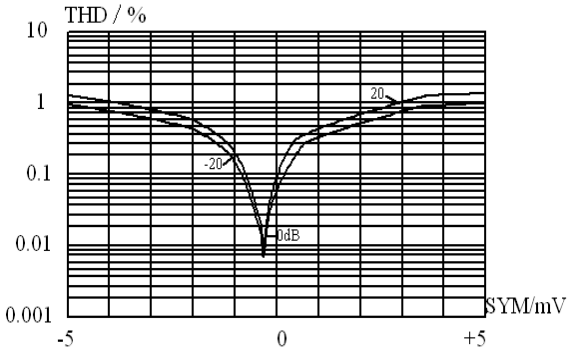


Figure 3. Typical THD Vs. Symmetry Voltage

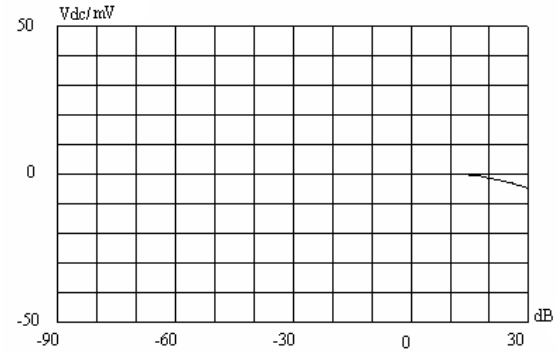


Figure 4. DC Offset Vs. Gain, After Symmetry Adjustment

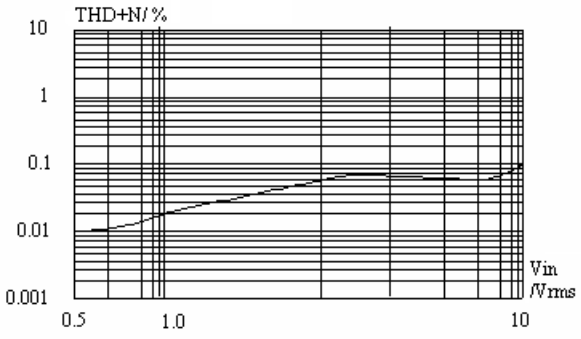


Figure 5. THD+Noise Vs. Input Level @1kHz, -15dB Gain

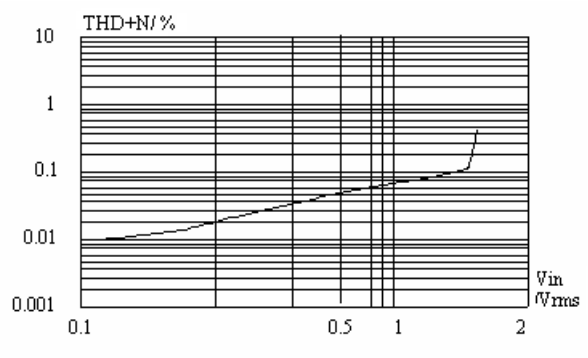


Figure 6. THD+Noise Vs. Input Level @1kHz, +15dB Gain

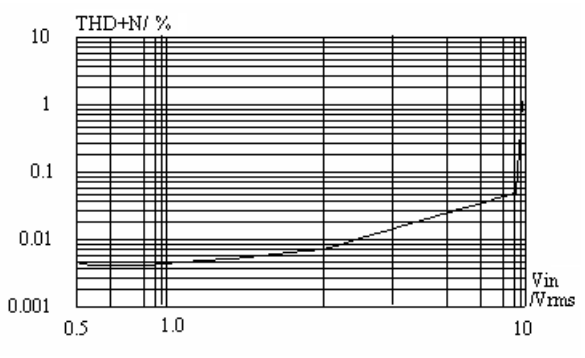


Figure 7. THD+Noise Vs. Input Level @1kHz, 0dB Gain

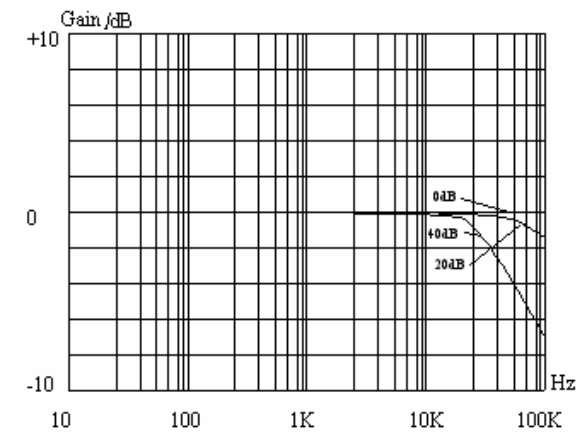


Figure 8. Gain Vs. Frequency Response

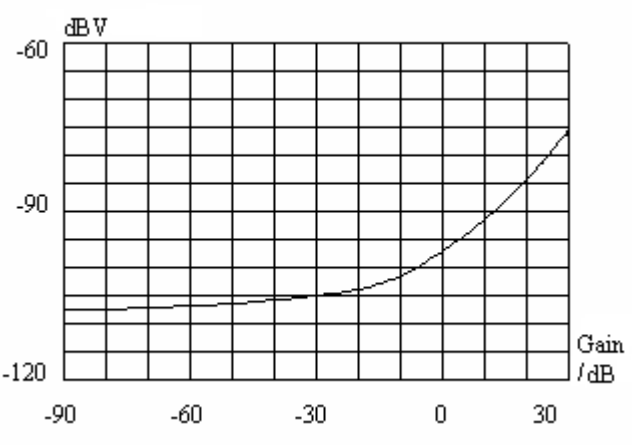


Figure 9. Noise (20kHz NBW) Vs. Gain

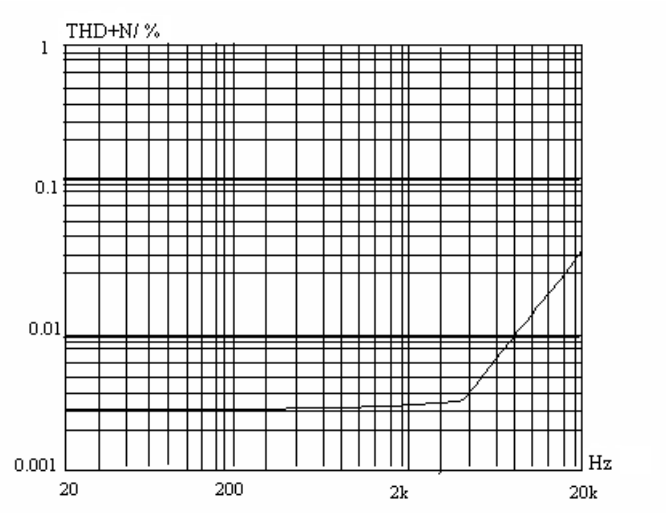


Figure 10. THD+Noise Vs. Frequency @ 0dB Gain

6、Typical Application Circuit and Information

6. 1、Application Circuit

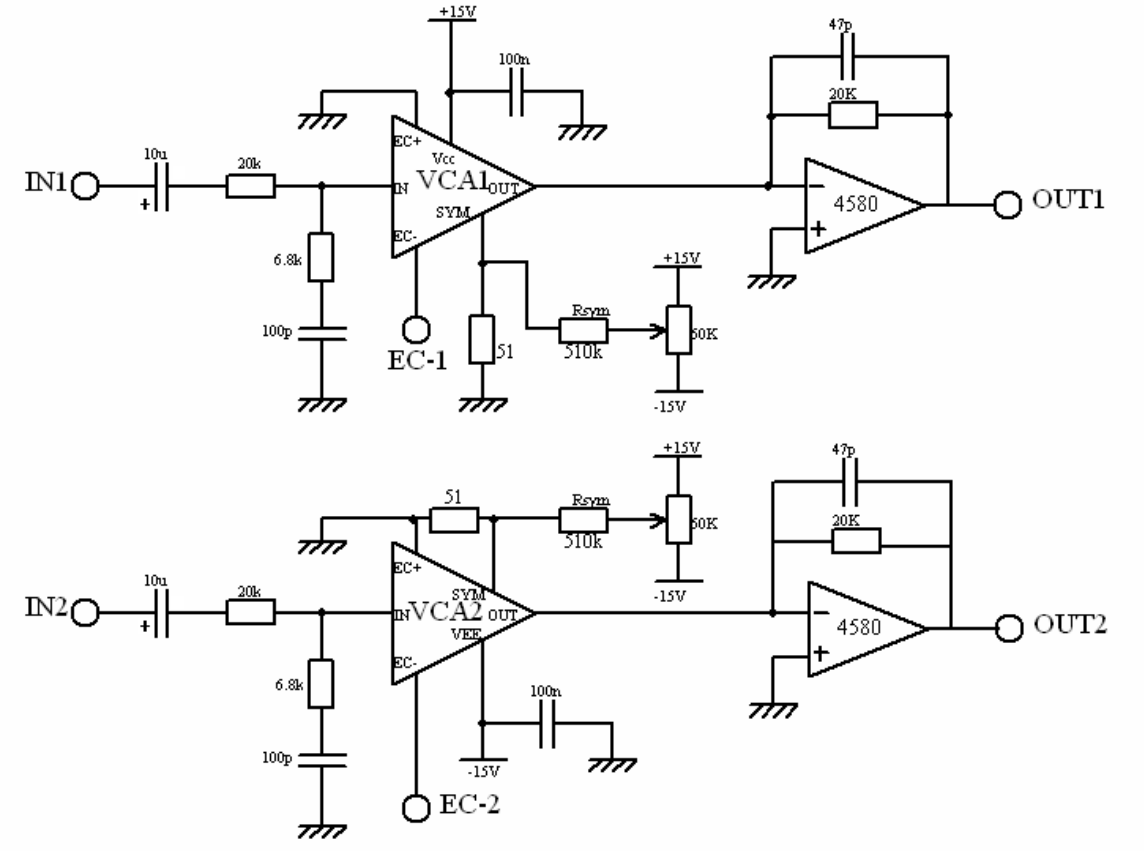


Figure 11. Typical Application Circuit

6. 2、Function Description and Applications Information

6.2.1、Theory of Operation

The V2162 VCA is designed for high performance in audio-frequency applications requiring exponential gain control, low distortion, wide dynamic range and low dc bias modulation. This part controls gain by converting an input current signal to a bipolar logged voltage, adding a dc control voltage, and re-converting the summed voltage back to a current through a bipolar antilog circuit.

Figure 12 presents a considerably simplified internal circuit diagram of the IC. The ac input signal current flows in the input pin. The internal op amp works to maintain the IN pin at a virtual ground potential. Q3/D3 and Q1/D1 act to log the input current, producing a voltage V3, which represents the bipolar logarithm of the input current. The voltage at the junction of D1 and D2 is the same as V3, but shifted by four forward V_{BE} drops.

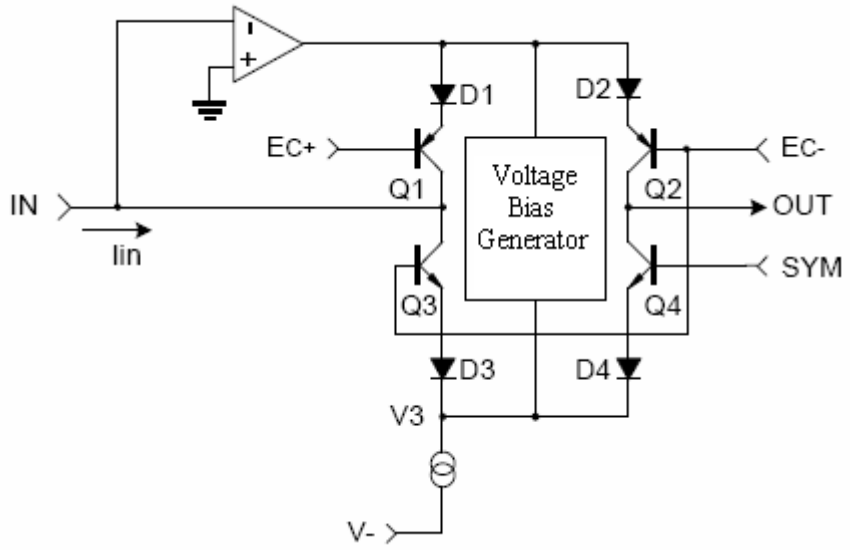


Figure 12. Simplified Internal Circuit Diagram

6.2.1.1、Positive Input Currents

For positive input currents (defined as currents flowing into the input pin), the op amp turns Q1 and D1 off, while simultaneously turns Q3 and D3 on. Thus, the input signal current is forced to flow through Q3 and D3.

6.2.1.2、Logging & Antifogging

Since the voltage across a base-emitter junction is logarithmic with collector, that is, $V_{BE}=V_T\ln（Ic/Is）$. The voltage from the base of Q3 to the cathode of D3 is proportional to the log of the positive input current. The voltage at the cathodes of D3 and D4 is therefore proportional to the positive input currents plus the voltage at EC- pin, the negative control port. Mathematically,

$V3=E_{C-}-2V_T\ln（I_{C3}/Is）$

Where V3 is the voltage at the junction of D3 and D4, V_T is the thermal voltage, (=kT/q), I_{C3} is the collector current of Q3, and I_S is the reverse-saturation current of Q3. It is assumed that D3 matches Q3 (and will be assumed that they match Q4 and D4, as well).

In typical applications (see Figure11, Typical Application Circuit), the SYM pin is connected to a voltage source at ground or nearly ground potential. The OUT pin is connected to a virtual ground. With these, the voltage at the cathodes of D3 and D4 will cause an exponentially-related current to flow in D4 and Q4, and output via the OUT pin. A similar equation governs this behavior:

$V3=E_{C+}-2V_T\ln（I_{C4}/Is）$

6.2.1.3、Exponential Gain Control

According to the two preceding equations:

$V3=E_{C-}-2V_T\ln（I_{C3}/Is）=E_{C+}-2V_T\ln（I_{C4}/Is）$

$E_{C+}-E_{C-}=2V_T\ln（I_{C4}/Is）-2V_T\ln（I_{C3}/Is）=2V_T\ln（I_{C4}/I_{C3}）$

Rearranging terms,

$I_{C4}=I_{C3}\cdot\exp[(E_{C+}-E_{C-})/2V_T]$

The ratio of currents is exponential with the difference in the voltages EC+ and EC-, providing convenient "decibel-linear" control. Mathematically, this is:

Av= I_{C4}/ I_{C3}= $e^{(EC+-EC-)/2VT}$, where A_V is the current gain.

For EC+ pin at or very near ground, at room temperature (25℃), converting the expression of A_V to a base of 10 for the exponential, this reduce to:

Av= $10^{-EC-/0.118}$

Another way of expressing this relationship is:
Gain=20logAv=-Ec-/0.0059, where Gain is the gain in decibels.

6.2.1.4、Negative Input Currents

For negative input currents, the operation of Q1/D1 and Q3/D3 is symmetric with Q2/D2 and Q4/D4. The EC+ pin is connected to ground, or very nearly ground potential (refer to the section 6.2.1.5 on symmetry adjustment for more detail), Since the top pair versus the bottom pair transistors are inverted (NPN/PNP) and the bases are cross-connected between the input (left) half and the output (right) half of each pair, the polarity (positive/negative, in dB) of the gain is the same.

6.2.1.5、Symmetry Adjustment

The layout design construction of the V2162 assures relatively good matching between the paired transistors, but even small V_{BE} mismatches will cause a dc output current to flow in the OUT pin, which will ultimately manifest itself as a dc offset voltage. The mismatch-caused dc output current will be modulated by gain commands, and may become audible as "thumps" if large, fast gain changes are commanded.

Transistor matching also affects distortion. If the top half of the gain cell is perfectly matched, while the bottom half is slightly off, then the gain commanded by the voltage at the EC- pin will affect the two halves of the core differently. Since positive and negative halves of ac input signals are handled by separate parts of the core, this gives rise to even-order distortion products.

For these reasons, the bases of Q1 and Q4 are brought out separately to the EC+ pin and the SYM pin, respectively. This allows a small static voltage differential to be applied to the two bases. The applied voltage must be set to equal the sum of the V_{BE} mismatches around the core. Figure 11 includes a typical circuit to apply this symmetry voltage. It controls primarily even-order harmonic distortion, and is usually adjusted for minimum THD at the output.

6.2.1.6、Opposite Polarity Control

As may be seen from the mathematics, the bases of Q1 (the EC+ pin) and Q4 (the SYM pin) can also be used as a control port, with an opposite sense of control from that at the EC- pin. To use this port, both pins must be driven with the control voltage, while a small differential voltage is accommodated between the two pins (Figure 13 shows the typical connection). Either the EC- pin, or the EC+ and SYM pins, or both ports together may be used for gain control. Mathematically, this relationship is as follows:

Av= $10^{(E_{C+}-E_{C-})/0.12}$, where Av is the gain in volt/volt, or Gain=20logAv=(E_{C+}-E_{C-})/0.006, where Gain is the gain in decibels.

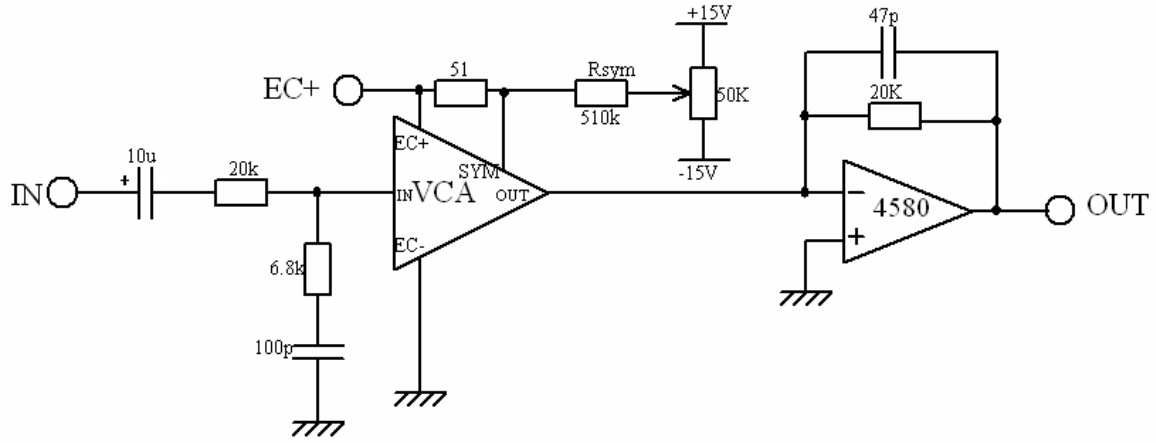


Figure 13. Positive Control Port Using Pins EC+ and SYM

6.2.1.7、DC Input Signals

Any dc currents in the feedback loop of the internal op amp will show up as dc terms in the output signal, and will be modulated by gain commands. Input bias currents will cause a dc current to flow in the feedback loop provided by the input side of the core. For this reason, input bias currents in the internal op amp must be kept very low. The bias current compensation at the input stage provides excellent cancellation of the bias current required by the input differential amplifier. To prevent dc current supplied from outside the VCA, ac input coupling is strongly recommended.

6.2.1.8、Headroom

Maximum signal currents are also limited by the logarithmic characteristics of the core transistors. The V2162 is specially constructed to conform to an ideal log-linear curve over a wide range of currents, but they reach their limit at approximately 1mA. The symptom of failing log conformance is increasing distortion with increasing current levels. Figure 5 through 7 show distortion versus signal level for -15dB, 0dB, and +15dB gain at the frequency of 1kHz. The acceptable distortion will determine the maximum signal level for a particular design.

6.2.2、Applications

6.2.2.1、Input

As mentioned above, input and output signals are currents, not voltages, the current input/output mode provides great flexibility in application.

As show in figure 12, internal negative feedback loop provides a virtual ground to the input pin. Within the linear range of the device, the input resistor (shown as 20kΩ in figure 11, the Typical Application Circuit) should be scaled to convert the available ac input voltage to a current. In order to obtain best distortion performance, peak input currents should be kept under 1mA. The input impedances must be less than 30kΩ to assure the circuit stability.

Since the feedback impedances around the internal op amp (essentially Q1/D1 and Q3/D3) are fixed, low values for the input resistor will require more closed-loop gain from the op amp. Since the open-loop gain naturally falls off at high frequencies, asking for too much gain will lead to increased high-frequency distortion. For best results, this resistor should be kept to 10kΩ or above. Distortion vs. frequency for a 1V signal at 0 dB gain with a 20 kΩ input

resistor is plotted in Figure 10.

As mentioned above, any dc input currents will cause dc signals in the output. The dc signals will be modulated by gain command, in turn causing audible thump. Therefore, capacitive coupling is almost mandatory for quality audio applications. Choose a capacitor which will give acceptable low frequency performance for the application.

6.2.2.2、Output

The output pin should be connected to a virtual ground node, so that current flowing in it may be converted to a voltage. Choose the external op amp can improve audio performance.

A small feedback capacitor around the output op amp is necessary to cancel the output capacitance of the VCA. Without it, this capacitance will destabilize most op amps. The capacitance at the OUT pin is typically 30pF.

6.2.2.3、Voltage Control

The EC- pin is the primary voltage control pin. This port controls gain inversely with applied voltage: positive voltage causes loss, negative voltage causes gain. The current gain of the VCA is unity when the EC- pin is at 0V and varies with voltage at approximately -6.0m/dB, at room temperature.

As implied by the equation for A_V, the gain is sensitive to temperature. The constant of proportionality is 0.33% of the decibel gain commanded, per degree Celsius, referenced to 27℃ (300K). The formula is:

$Gain=(E_{C+}-E_{C-})/(0.006\times1.0033\times\triangle T)$

Where E_C is in volts, and $\triangle T$ is the difference between the actual temperature and room temperature (27℃)

For most audio applications, this change with temperature is of little consequence. However, if necessary, it may be compensated by a resistor which varies its value by 0.33%/℃.

When the EC- pin is used for voltage control, the EC+ pin is connected to ground and the SYM pin is used to apply a small symmetry voltage (~±4 mV) to correct for V_{BE} mismatches within the VCA. Therefore, in order to obtain optimum performance, the SYM pin connects with an external impedance of approximately 50Ω. A trim pot is used to adjust the voltage between the EC+ pin and the SYM pin as shown in Figure 11 (Typical Application Circuit). Voltage adjustment range is ±4 mV.

The EC+ pin and the SYM pin can be used together as an opposite sense voltage control port. A typical circuit using this approach is shown in Figure 13. The EC- pin may be grounded and the EC+ pin driven against the symmetry-adjustment voltage. The change in voltage at the EC+ pin does have a small effect on the symmetry voltage, but this is of little practical consequence in most applications.

It is also possible (and advantageous) to combine both controls with differential drive (see Figure 14). While the driving circuitry is more complex, this configuration offers better performance at high attenuation levels (<-90dB) where the single control port circuits begin to saturate Q1 (for E_{C+} drive) or Q3 (for E_{C-} drive). When either of these transistors saturates, the internal op amp will accommodate the change in current demand by responding with a small change in its input offset voltage. This leads to an accumulation of charge on the input capacitor, which in turn can cause thump when the high attenuation is suddenly removed (e.g.,

when a muted channel is opened). Differential control drive avoids the large dc levels otherwise required to command high attenuation. (+600 mV for -100dB gain at the EC- pin alone, vs. ±300 mV when using both the EC- pin and the EC+ pin).

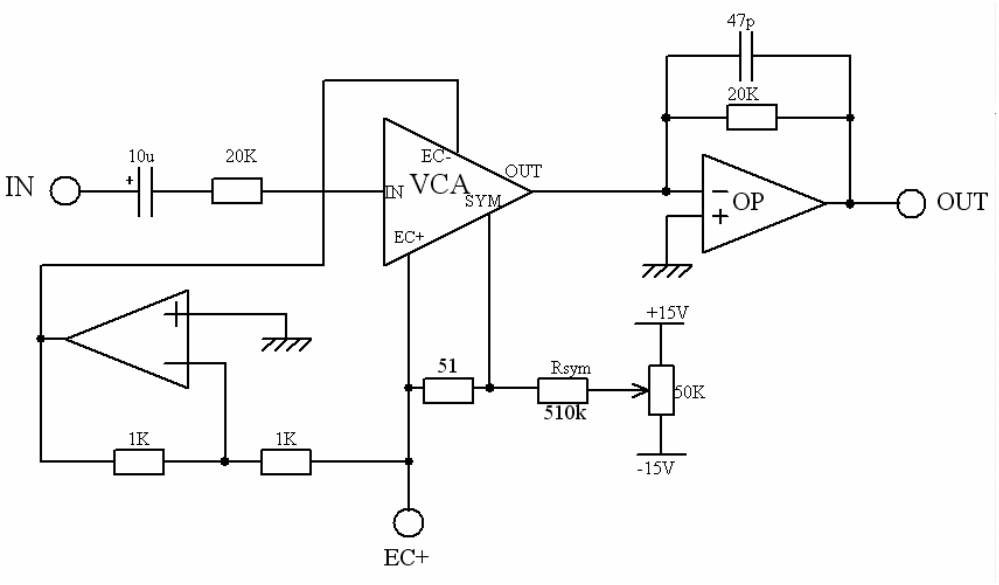


Figure 14. Using Both Control Ports

6.2.2.4、Control Port Drive Impedance

The control port should be driven by a low source impedance for minimum distortion. This often suggests driving the control port directly with an op amp (see section 6.2.2.5 below, Noise Considerations). However, the closed-loop output impedance of an op amp typically rises at high frequencies due to falling loop gain. The output impedance is therefore inductive at high frequencies. Excessive inductance in the control port source impedance can cause the VCA to oscillate internally. In such cases, a 100Ω resistor in series with a 1.5nF capacitor between the control port and ground will usually suffice to prevent the instability.

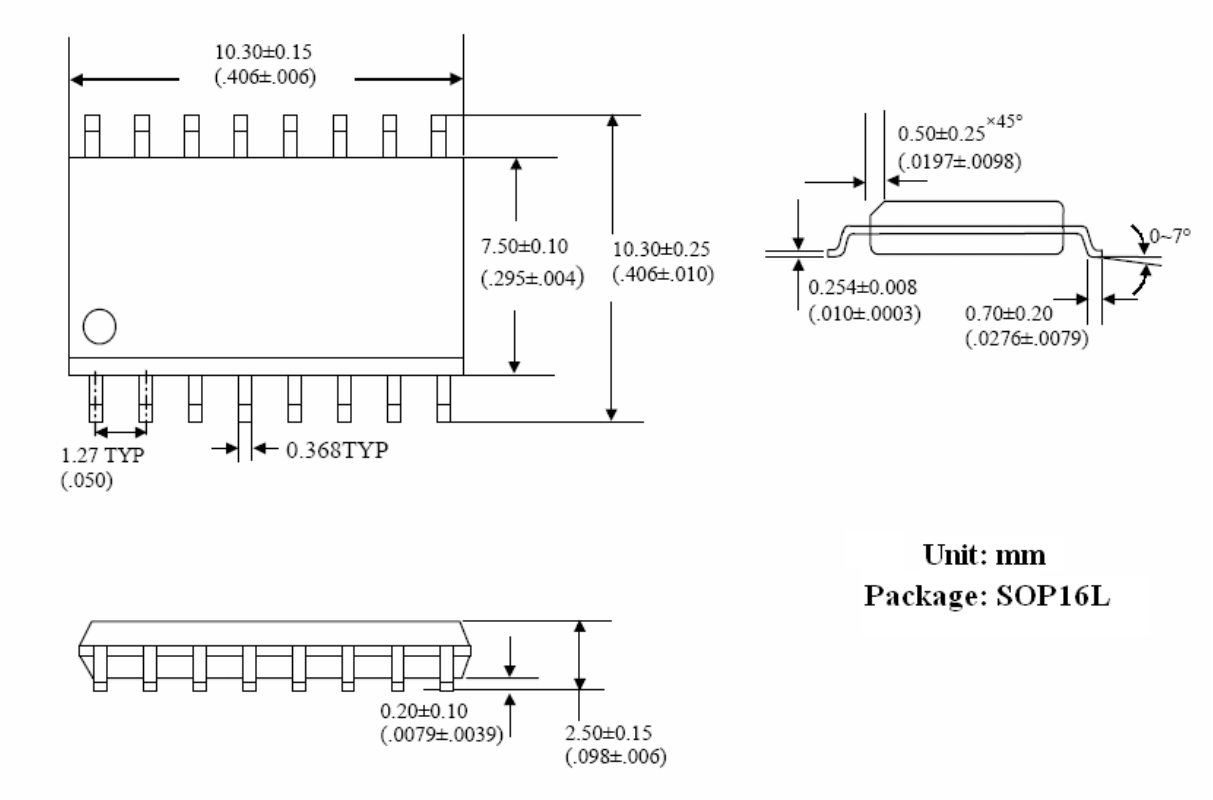
6.2.2.5、Noise Considerations

For good audio designers, it is important to consider the effects of noisy devices on the signal path. As is well known, this includes not only active devices, but also impedance. High value resistors have inherent thermal noise. And the wrong choice of impedance levels will easily bring on the noise performance of an otherwise quiet circuit being spoiled.

However, the effect of noisy circuitry and high impedance levels in the control path of voltage-control circuitry is easily neglected. The V2162 VCA act like double-balanced multipliers: when no signal is present at the signal input, noise at the control input is rejected. So, when measuring noise (in the absence of signal, as most everyone does), even very noisy control circuitry often goes unnoticed. However, noise at the control port of these parts will cause noise modulation of the signal. This can become significant if care is not taken to drive the control ports with quiet signals.

Quiet electronics throughout the control-voltage circuitry can be used to avoid excessive noise. One useful technique is to process control voltages at a multiple of the eventual control constant (e.g., -60mV/dB, ten times higher than the VCA requires). And then attenuate the control signal just before the final drive amplifier. With careful attention to impedance levels, relatively noisy op amps may be used for all but the final stage.

7、Package Dimensions



Unit: mm

Package: SOP16L