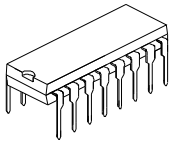
V571D/M LINEAR INTEGRATED CIRCUIT

COMPANDER

DESCRIPTION

The V571D/M is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full-wave rectifier to detect the average value of the signal, a linerarized temperature-compensated variable gain cell, and an operational amplifier.

The V571D/M is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio systems.



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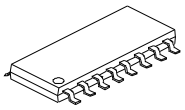


SOP-16

APPLICATIONS

- Cellular radio
- High level limiter
- Low level expandor—noise gate
- Dynamic filters
- CD Player

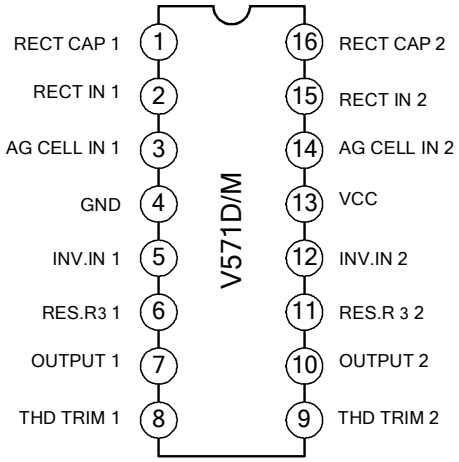
ORDERING INFORMATION

V571D	DIP-16-300-2.54
V571M	SOP-16-375-1.27

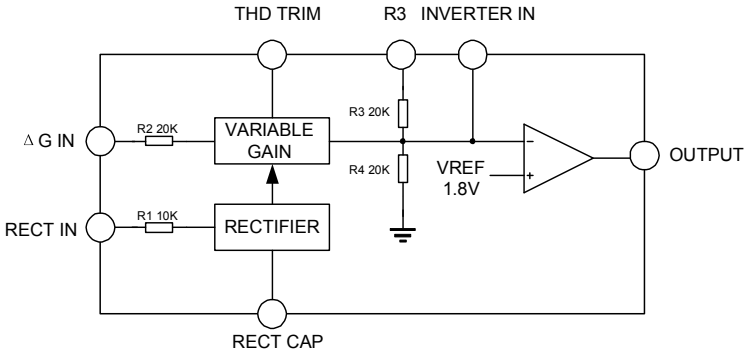
FEATURES

- Complete compressor and expandor in one IChip
- Temperature compensated
- Greater than 110dB dynamic range
- Operates down to 6VDC
- System levels adjustable with external components
- Distortion may be trimmed out
- Dynamic noise reduction systems
- Voltage-controlled amplifier

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Characteristic	Symbol	Value	Unit
Maximum Operating Voltage	V_{CC}	18	V
Operating Temperature	T_A	0~70	°C
Power dissipation	P_D	400	mW

AC ELECTRICAL CHARACTERISTICS (Ta=25°C, Vcc=+6V,unless otherwise stated)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}		6		18	v
Supply Current	I_{CC}	No signal		3.2	4.8	mA
Output Current capability	I_{OUT}		±20			mA
Output Slew Rate	SR			±.5		V/μs
Gsin Cell Distortion		Untrimmed Trimmed		0.5 0.1	2.0	%
Resister Tolerance				±5	±15	%
Internal Reference Voltage			1.7	1.85	2.0	V
Output DC Shift		Untrimmed		±30	±150	mV
Expandor Output Noise		No signal, 15Hz-20kHz		20	60	μV
Unity Gain Level		1kHz	-1.5	0	+1.5	dBm
Gain Change				±0.1		dB
Reference Drift				+2,-25	+20,-50	mV
Resistor Drift				+8,-0		%
Tracking Error(measured relative to value at unity gain) Equals [VO-VO(unity gain)]dB-V2dBm		Rectifier input, V2=+6dBm,V1=0dB V2=-30dBm, V1=0dB		+0.2 +0.2	-1,+1.5	dB
Channel Separation				60		dB

Note: 1. Input to V 1 and V 2 grounded.

2. Measured at 0dBm, 1kHz.

3. Expandor AC input change from no signal to 0dBm.

4. Relative to value at T A = 25°C.

5. Electrical characteristics for the V571D/M only are specified over -40 to +8 °C temperature range.

6. 0dBm = 775mV RMS .

FUNCTION DESCRIPTION

CIRCUIT DESCRIPTION

The V571D/M compandor building blocks, as shown in the block diagram, are a full-wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full-wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively-coupled voltage inputs as shown in the following equation. Note that for capacitively-coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|_{avg}}{R1} \text{ or}$$

$$G \propto \frac{|V_{IN}|_{avg}}{R1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expander or compressor application, this would lead to third harmonic distortion, so there is a trade-off to be made between fast attack and decay times and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t)=(G_{initial}-G_{final})e^{-t/\tau}+G_{final};\ \tau=10k \times C_{RECT}$$

The variable gain cell is a current-in, current-out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the DG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively-coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R2} = \frac{V_{IN}}{R2}$$

A compensation scheme built into the DG cell compensates for temperature and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

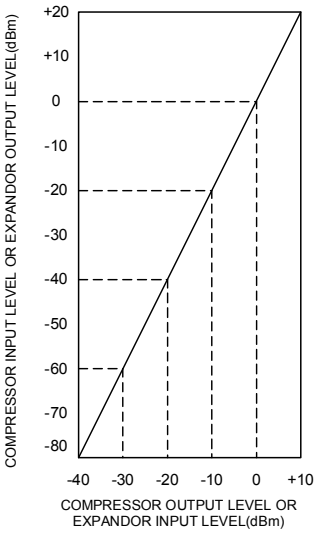
The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the DG cell output as well as brought out externally. A resistor, R 3 , is brought out from the summing node and allows compressor or expander gain to be determined only by internal components.

The output stage is capable of ±20mA output current. This allows a +13dBm ($3.5V_{RMS}$) output into a 300W load

which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

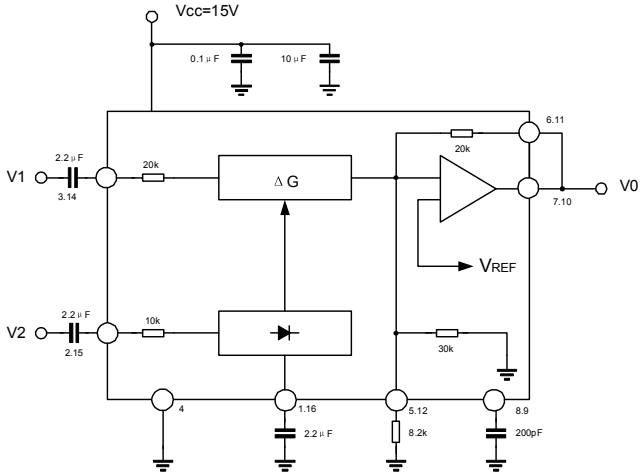
A bandgap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and DG cell, and a bias current for the DG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expander circuits.



Basic Input-Output Transfer Curve

TYPICAL TEST CIRCUIT



Typical Test Circuit

INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high-performance is required, one has to resort to complex discrete circuitry with many expensive, well-matched components.

This paper describes an inexpensive integrated circuit, the V571D/M Compandor, which offers a pair of high performance gain control circuits featuring low distortion (<0.1%), high signal-to-noise ratio (90dB), and wide dynamic range (110dB).

CIRCUIT BACKGROUND

The V571D/M Compandor was originally designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal-to-noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 1 graphically shows what a compandor can do for the signal-to-noise ratio of a restricted dynamic range channel. The input level range of +20 to -80dB is shown undergoing a 2-to-1 compression where a 2dB input level change is compressed into a 1dB output level change by the compressor. The original 100dB of dynamic range is thus compressed to a 50dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45dB.

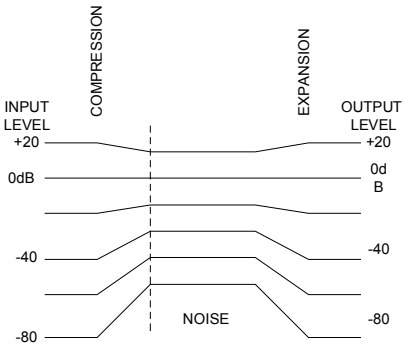


Figure 1. Restricted Dynamic Range Channel

The significant circuits in a compressor or expander are the rectifier and the gain control element. The phone system requires a simple full-wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized Tran conductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. These features make the circuit useful in audio and data systems as well as in telecommunications systems.

BASIC CIRCUIT HOOK-UP AND OPERATION

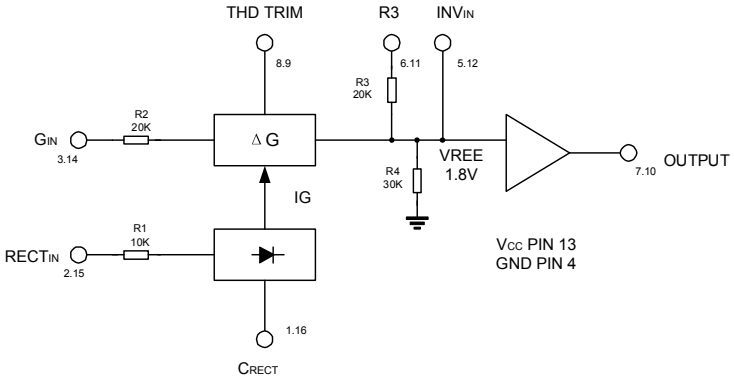


Figure 2. Chip Block Diagram

Figure 2 shows the block diagram of one half of the chip, (there are two identical channels on the IC). The full-wave averaging rectifier provides a gain control current, I_G , for the variable gain (ΔG) cell. The output of the DG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output DC bias.

The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8V reference denoted V_{REF} . The non-inverting input of the op amp is tied to V_{REF} , and the summing nodes of the rectifier and ΔG cell (located at the right of R1 and R2) have the same potential. The THD trim pin is also the V_{REF} potential.

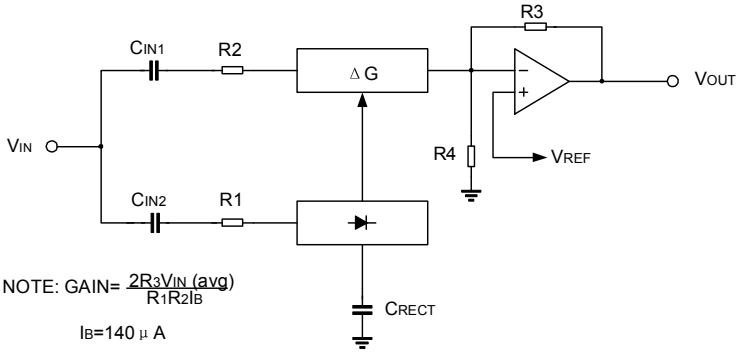


Figure 3. Basic Expander

Figure 3 shows how the circuit is hooked up to realize an expandor. The input signal, V_{IN} is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6dB, the gain control current will drop by a factor of 2, and so the gain will drop 6dB. The output level at V_{OUT} will thus drop 12dB, giving us the desired 2 to 1 expansion.

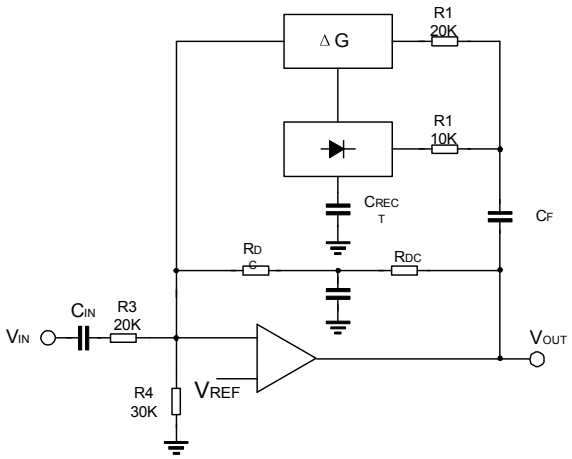


Figure 4. Basic Components

Figure 4 shows the hook-up for a compressor. This is essentially an expandor placed in the feedback loop of the op amp . the ΔG cell is setup to provide AC feedback only, so a separate DC feedback loop is provide by the two R_{DC} and C_{DC}. The values of R_{DC} will determine the DC bias at the output of the amp. The output will bias to:

$$V_{OUT}DC = 1 + \frac{R_{DC1} + R_{DC2}}{R_4}$$

$$V_{REF} = (1 + \frac{R_{DCTOT}}{30K})1.8V$$

The output of the expander will bias up to:

$$V_{OUT}DC = 1 + \frac{R_3}{R_4}V_{REF}$$

$$V_{REF} = (1 + \frac{20K}{30K})1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistor are used. External resistor may be placed in series with r3, (which will affect the gain), or in parallel with r4 to raise the DC bias to any desired value.

CIRCUIT DETAILS—RECTIFIER

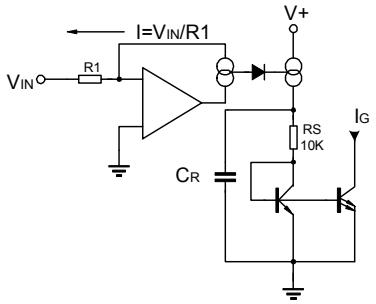


Figure 5. Rectifier Concept

Figure 5 shows the concept behind the full-wave averaging rectifier. The input current to the summing node of the op amp, V_{IN} R 1 , is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R5 , CR, which set the averaging time constant, and then mirrored with a gain of 2 to become I_G , the gain control current.

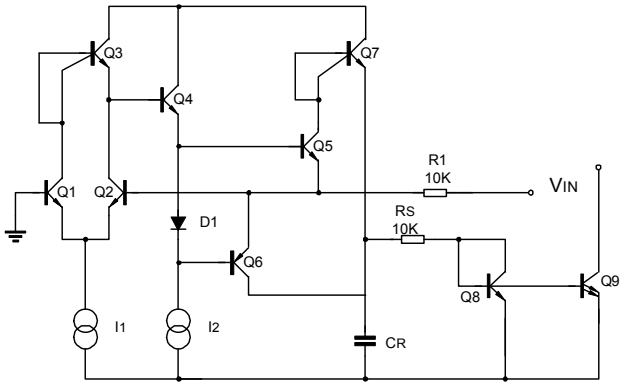


Figure 6. Simplified Rectifier Schematic

Figure 6 shows the rectifier circuit in more detail. The op amp is a one-stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q 1), which is shown grounded, is actually tied to the internal 1.8V V_{REF} . The inverting input is tied to the op amp output, (the emitters of Q 5 and Q 6), and the input summing resistor R 1 . The single diode between the bases of Q 5 and Q 6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q 5 and Q 6 . Q 6 will conduct when the input swings positive and Q 5 conducts when the input swings negative. The collector currents

will be in error by the a of Q 5 or Q 6 on negative or positive signal swings, respectively. ICs such as this have typical NPN bs of 200 and PNP bs of 40. The a's of 0.995 and 0.975 will produce errors of 0.5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere 0.13dB gain error.

At very low input signal levels the bias current of Q 2 , (typically 50nA), will become significant as it must be supplied by Q 5 . Another low level error can be caused by DC coupling into the rectifier. If an offset voltage exists between the V IN input pin and the base of Q 2 , an error current of V_{OS} /R 1 will be generated. A mere 1mV of offset will cause an input current of 100nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the PNP Q 6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250mA. If necessary, an external resistor may be placed in series with R 1 to limit the current to this value. Figure 7 shows the rectifier accuracy vs input level at a frequency of 1kHz.

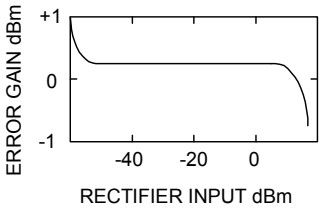


Figure 7. Rectifier Accuracy

At very high frequencies, the response of the rectifier will fall off. The roll-off will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q 5 or Q 6 conducting. The rectifier frequency response for input levels of 0dBm, -20dBm, and -40dBm is shown in Figure 8. The response at all three levels is flat to well above the audio range.

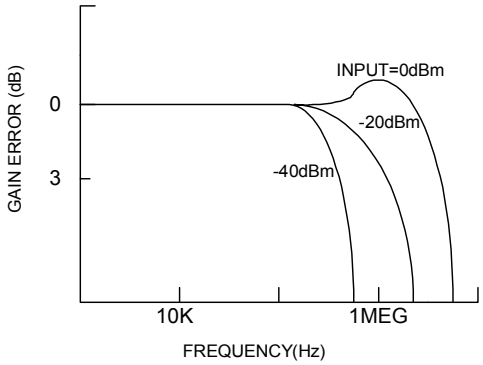
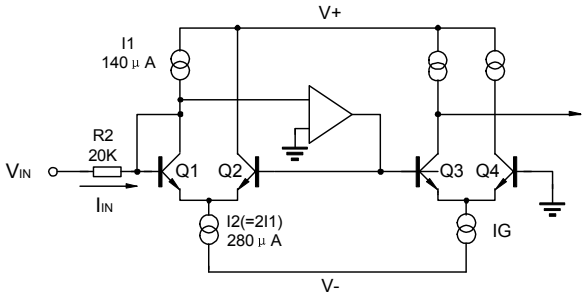


Figure 8. Simplified ΔG Cell Schematic

VARIABLE GAIN CELL



Note: $L_{OUT} = \frac{LG}{L1} IIN = \frac{IGVIN}{I2R2}$

Figure 9. Simplified ΔG Cell Schematic

Figure 9 is a diagram of the variable gain cell. This is a linearized two-quadrant transconductance multiplier. Q 1 , Q 2 and the op amp provide a predistorted drive signal for the gain control pair, Q 3 and Q 4 . The gain is controlled by I G and a current mirror provides the output current.

The op amp maintains the base and collector of Q 1 at ground potential (V_{REF}) by controlling the base of Q 2 . The input current I_{IN} ($=V_{IN}/R\ 2$) is thus forced to flow through Q 1 along with the current I 1 , so $I_{C1} = I_1 + I_{IN}$. Since I_2 has been set at twice the value of I_1 , the current through Q 2 is:

$$I_2 - (I_1 + I_{IN}) = I_1 - I_{IN} = I_{C2}.$$

The op amp has thus forced a linear current swing between Q 1 and Q 2 by providing the proper drive to the base of Q 2 . This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the non-linearity of the differential pair, Q 1 and Q 2 , under large signal conditions.

The key to the circuit is that same predistorted drive signal is applied to the gain control pair, Q3 and Q4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical regardless of the magnitude of the currents. This gives us :

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1 + I_{IN}}{I_1 - I_{IN}}$$

plus the relationships $I_G = I_{C3} + I_{C4}$ and $I_{OUT} = I_{C4} - I_{C3}$ will yield the multiplier transfer function,

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{V_{IN} I_G}{R_2 I_1}$$

This equation is liner and temperature-insenstive, but it assumes ideal transistor.

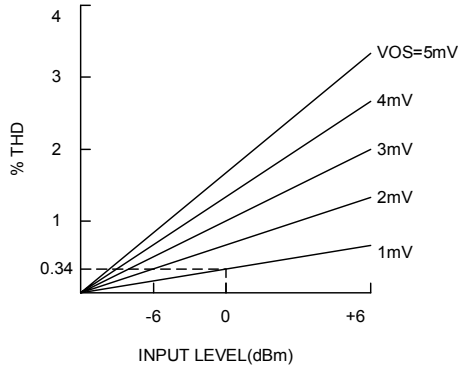


Figure 10. ΔG Cell Distortion vs Offset Voltage

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in second harmonic distortion. Figure 10 gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mV offset will yield 0.34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about mV. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 11 shows the simple trim network required.

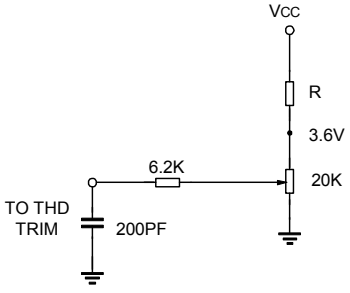


Figure 11. THD Trim Network

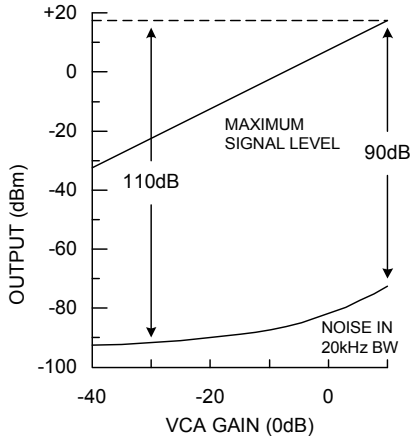


Figure 12. Dynamic Range of V571D/M

Figure 12 shows the noise performance of the DG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20dB of gain reduction. At high gains, the signal to noise ratio is 90dB, and the total dynamic range from maximum signal to minimum noise is 110dB.

Control signal feedthrough is generated in the gain cell by imperfect device matching and mismatches in the current sources, I 1 and I 2 . When no input signal is present, changing I G will cause a small output signal. The distortion trim is effective in nulling out any control signal feedthrough, but in general, the null for minimum feedthrough will be different than the null in distortion. The control signal feedthrough can be trimmed independently of distortion by tying a current source to the DG input pin. This effectively trims I . Figure 17 shows such a trim network.

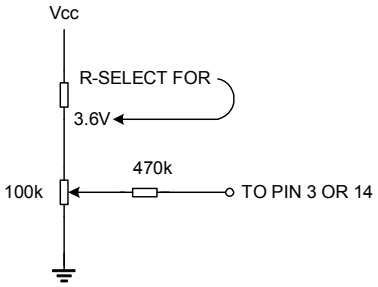


Figure 13. control Signal Feedthrough

OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1MHz bandwidth. Figure 18 shows the basic circuit. Split collectors are used in the input pair to reduce g M , so that a small compensation capacitor of just 10pF may be used. The output stage, although capable of output currents in excess of 20mA, is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

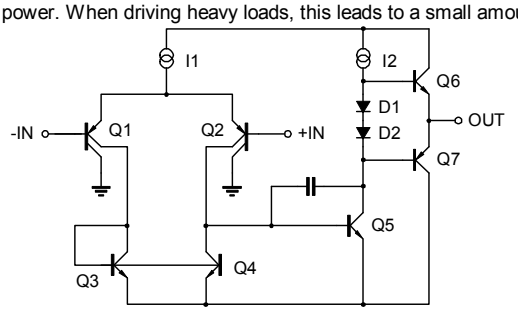


Figure 14. Operational Amplifier

RESISTORS

Inspection of the gain equations in Figures 3 and 4 will show that the basic compressor and expander circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hook-ups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 15 shows the effects of temperature on the diffused resistors which are normally used in integrated circuits, and the ion-implanted resistors which are used in this circuit. Over the critical 0°C to +70°C temperature range, there is a 10-to-1 improvement in drift from a 5% change for the diffused resistors, to a 0.5% change for the implemented resistors. The implanted resistors have another advantage in that they can be made the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.

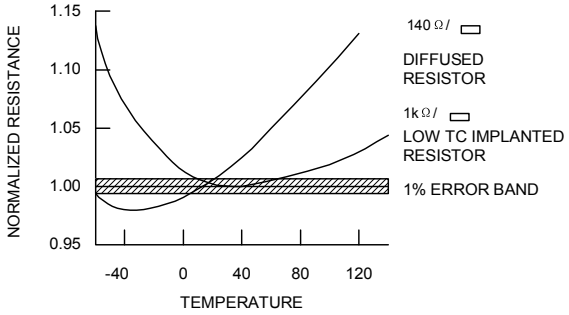
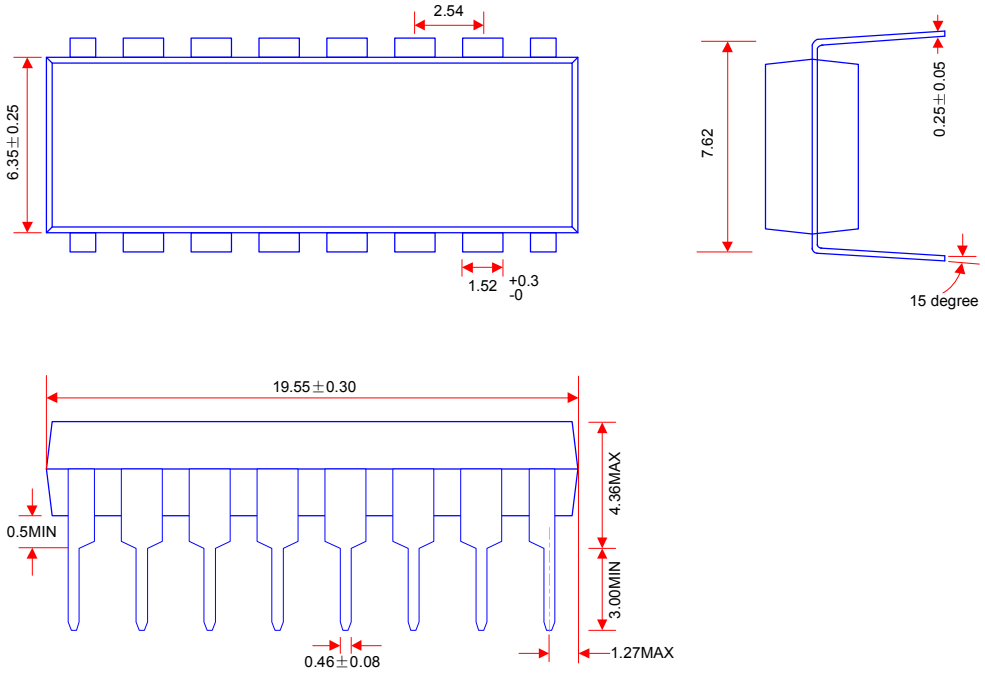


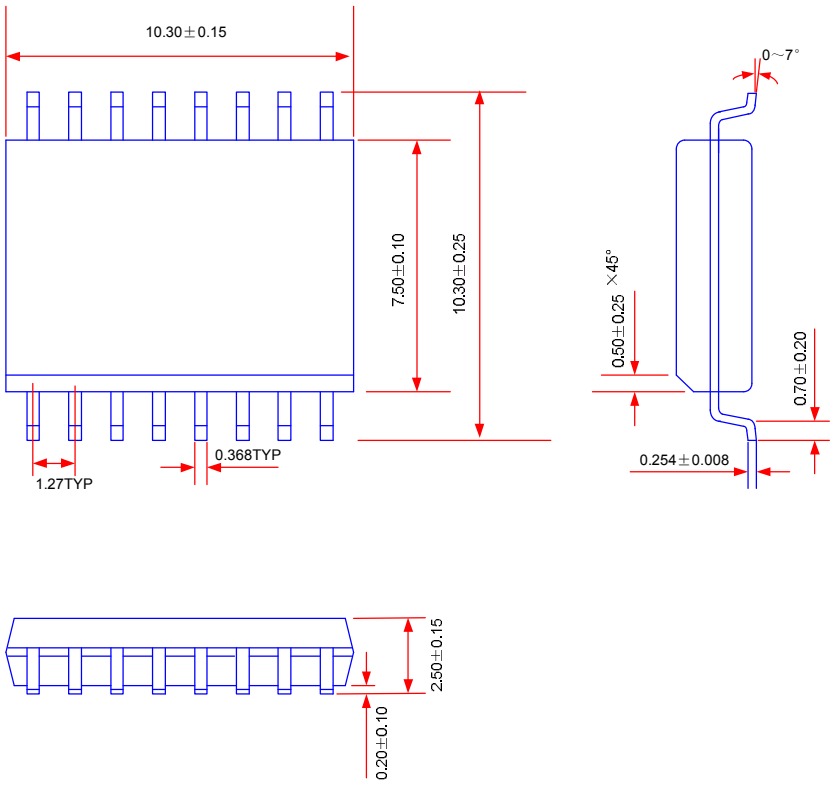
Figure 15. Resistance vs temperature

PACKAGE OUTLINE

DIP-16-300-2.54 UNIT: mm

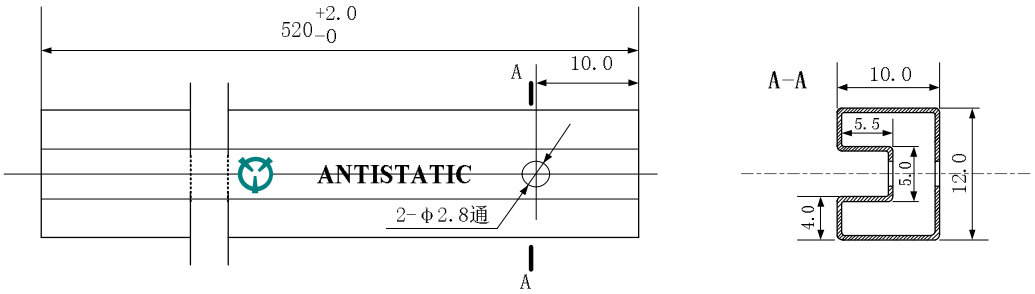


SOP-16-375-1.27 UNIT: mm



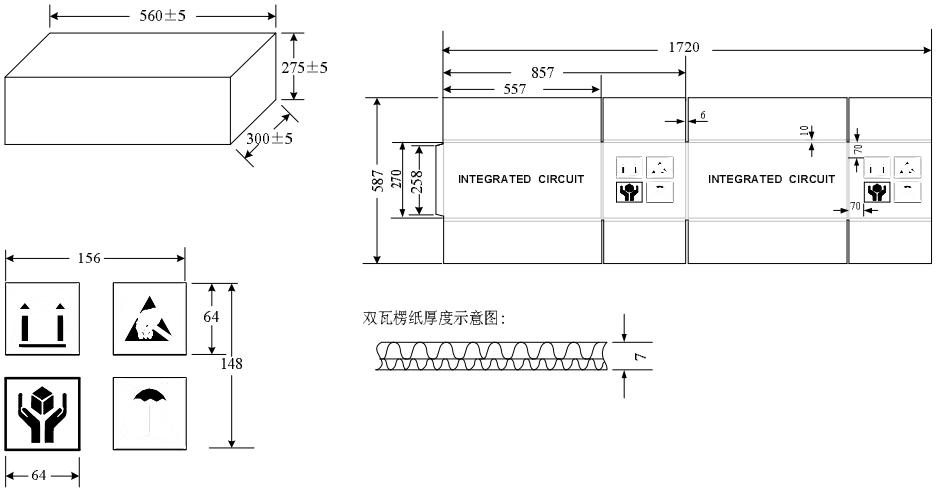
V571D STICK PACKAGE GRAPHICS (UNIT: mm)	DATE	2008-07-11
	MADE BY	
	AUDITOR	
	APPROVED BY	

1.STICK



STICK (DIP-16)

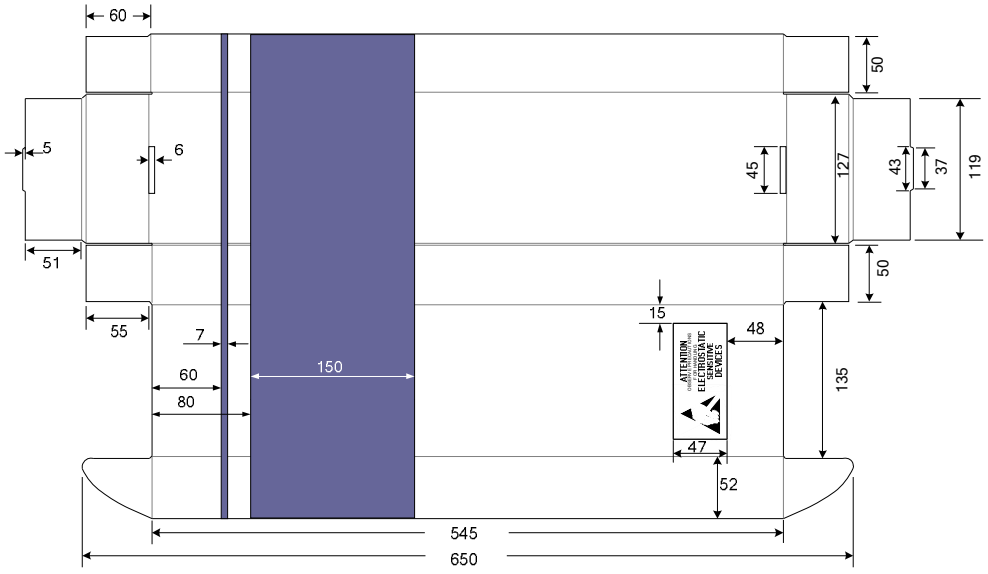
2.BOX1

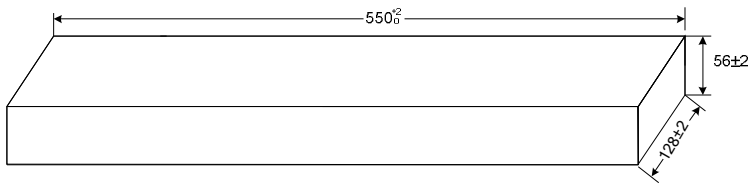


BOX 1

V571D STICK PACKAGE GRAPHICS (UNIT: mm)	DATE	2008-07-11
	MADE BY	
	AUDITOR	
	APPROVED BY	

3.BOX2





BOX 2

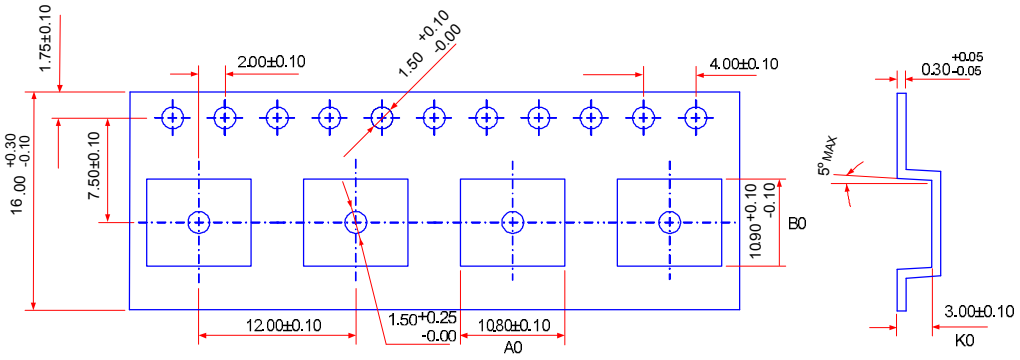
	STICK	BOX		
Package Format	Pcs /Stick	PCS/BOX2	BOX2 /BOX1	PCS /BOX1
DIP-16	25	1000	10	10000

4、GREEN-MARK

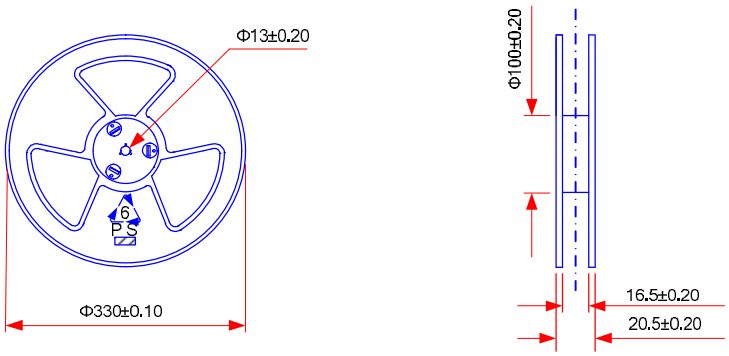
"Pb-FREE" label attached on the side of the BOX2 and attached above the bar code outside of the BOX1.

V571M T&R PACKAGE GRAPHICS (UNIT: mm)	DATE	2008-07-11
	MADE BY	
	AUDITOR	
	APPROVED BY	

1.TAPE

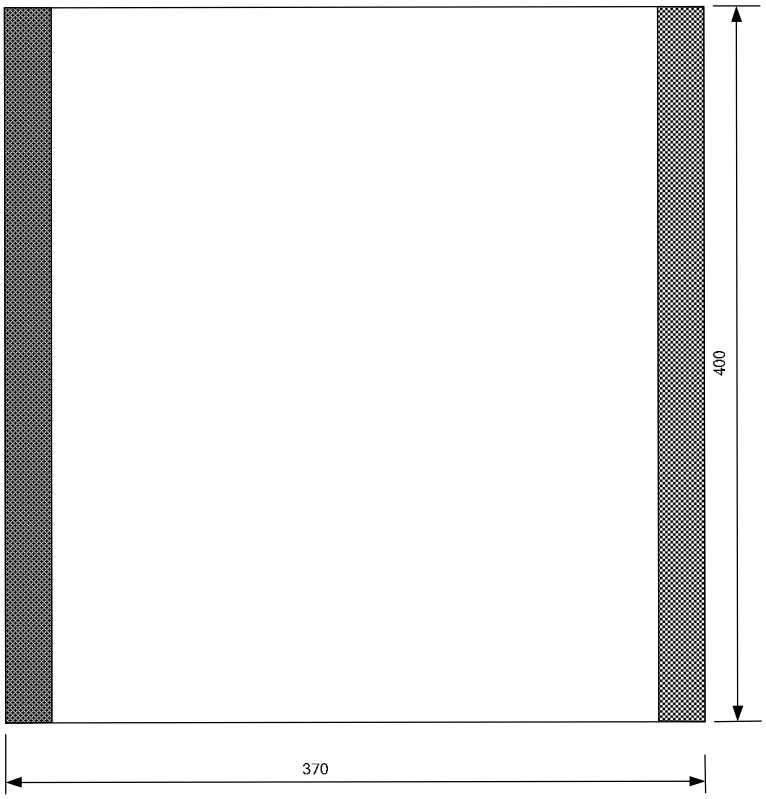


2.REEL



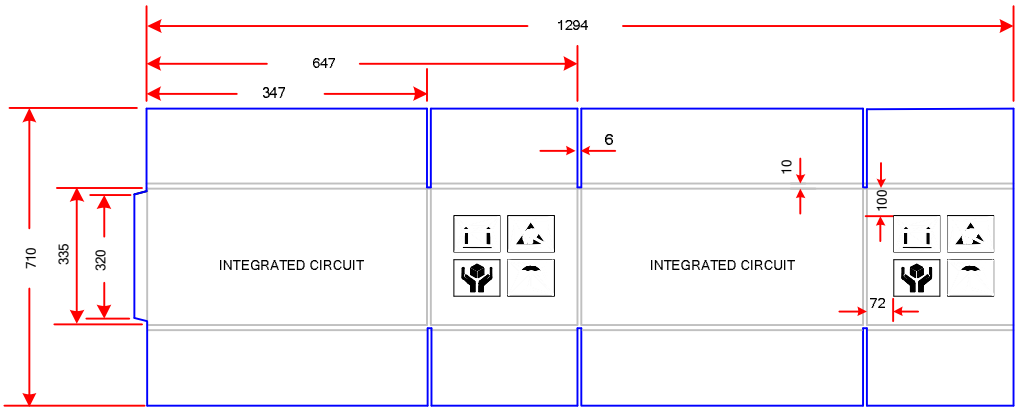
V571M T&R PACKAGE GRAPHICS (UNIT: mm)	DATE	2008-07-11
	MADE BY	
	AUDITOR	
	APPROVED BY	

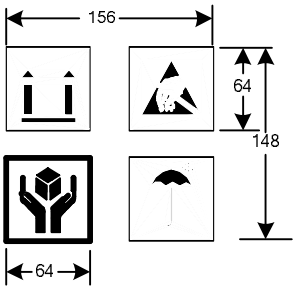
3. PLASTIC POCKET

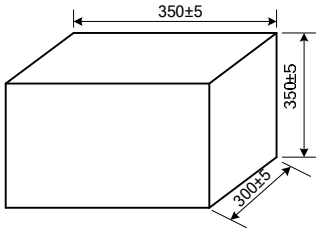


V571M T&R PACKAGE GRAPHICS (UNIT: mm)	DATE	2008-07-11
	MADE BY	
	AUDITOR	
	APPROVED BY	

4.BOX 1



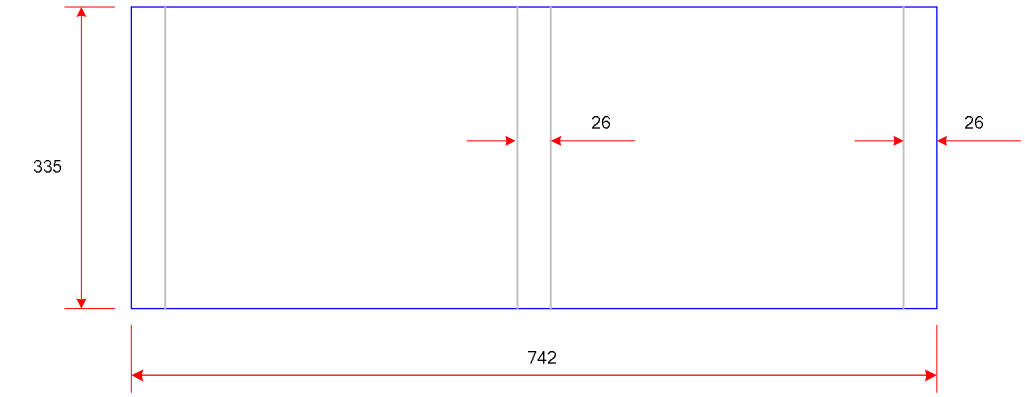


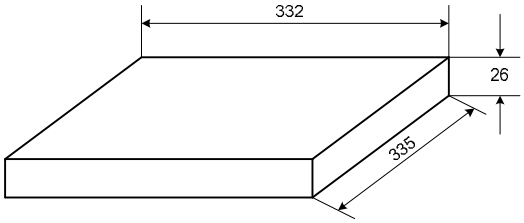


BOX 1

V571M T&R PACKAGE GRAPHICS (UNIT: mm)	DATE	2008-07-11
	MADE BY	
	AUDITOR	
	APPROVED BY	

5.BOX 2





	REEL	BOX		
Package Format	Pcs /REEL	Reel/BOX2	BOX2 /BOX1	PCS /BOX1
SOP-16	1500	1	10	15000

6、GREEN-MARK

"Pb-FREE" lable attached on the side of Plastic Pocket and attached above the bar code outside of the BOX2 .

V571D BILL OF MATERIAL	DATE	2008-07-11
	MADE BY	
	AUDITOR	
	APPROVED BY	

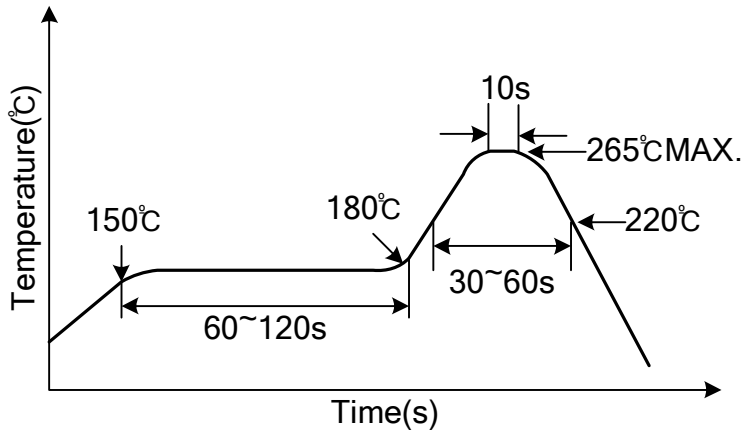
Name of the part	Material weight (mg/unit)	Material name	Material analysis (element)	Material analisys (weight%)
Lead Frame	**412.35**	**194**	**Fe** **Zn** **P** **Cu**	**2.2017%** **0.1052%** **0.0209%** **97.6722%**
Plastic	**656**	**Epoxy resin**	**SiO2** **Epoxy** **酚醛** **Brominated resin** **carbon black** **wax** **flame retardant** **catalyst** **stress absorbent** **coupling agent** **releasing agent**	**70-80%** **10-15%** **7-10%** **1%-2%** **0.1%-1%** **0.5%-2%** **1%-5%** **<1%** **<5%** **<1%** **<1%**
Chip	**1**	**Doped Silicon**		**>99%**
Die Attach Material	**0.45**	**Glue**	**Ag** **Epoxy resin**	**75%** **25%**
Wires	**0.2**	**Gold**	**Au**	**>99.99%**
Leads finishing	**10**	**Lead-Free**	**Pb＜100ppm**	

V571M BILL OF MATERIAL	DATE	2008-07-11
	MADE BY	
	AUDITOR	
	APPROVED BY	

Name of the part	Material weight (mg/unit)	Material name	Material analysis (element)	Material analisys (weight%)
Lead Frame	**74.89**	**C194**	**Fe** **Zn** **P** **Cu**	**2.1%-2.6%** **0.05%-0.2%** **0.015%-0.15%** **RAL**
Plastic	**98.94**	**KL-400-1T**	**Silica** **Epoxy resin** **Phendic Resin(Handener)** **Brominated resin** **Carbon Black** **Wax** **Flame Retardant** **Catalyst** **Stress Absorbent** **Coupling Agent** **Releasing Agent**	**70%-80%** **10%-15%** **7%-10%** **1%-2%** **0.1%-1%** **0.5%-2%** **1%-5%** **<1%** **<5%** **<1%** **<1%**
Die Attach Material	**0.315**	**DAD-90**	**NA**	**NA**
Wires	**0.2225**	**Gold**	**Au**	**99.99%**
Leads finishing	**7.725**	**Tin**	**Sn**	**99.90%**

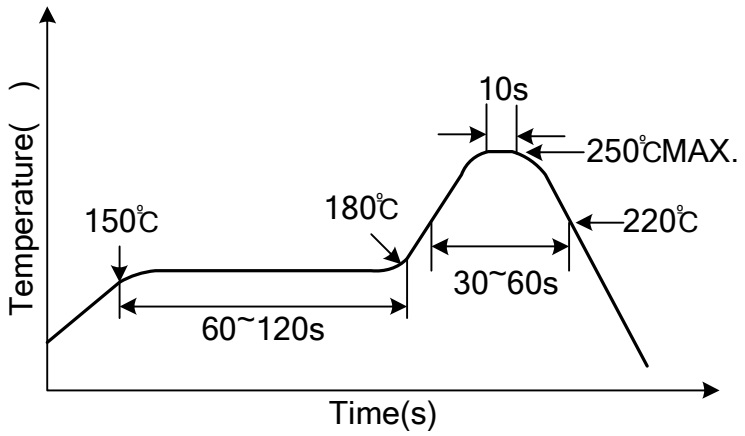
V571D/M INFRARED REFLOW SOLDERING CONDITION (SUGGESTION)	DATE	2008-07-11
	MADE BY	
	AUDITOR	
	APPROVED BY	

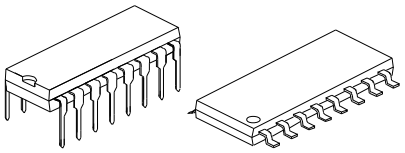
MAX. Temperature (Surface)	:	Below 265℃
MAX. Temperature Duration	:	≤10s
Above 220℃ Duration	:	30-60s
Between 150℃ and 180℃ Duration	:	60-120s
Soldering Times	:	2 Times



V571D/M WAVE SOLDERING CONDITION (SUGGESTION)	DATE	2008-07-11
	MADE BY	
	AUDITOR	
	APPROVED BY	

MAX. Temperature (Surface)	:	Below 250℃
MAX. Temperature Duration	:	≤10s
Pre-heat Temperature	:	120℃
Soldering Times	:	1 Times



Package form	
DIP-16-300 & SOP-16-375