M9000

120-dB, 192kHz Multibit DAC with Volume Control

Product Specification

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1. General Description and Features

The M9000 is a complete stereo 24 bit/192 kHz digital to-analog system. This D/A system includes digital deemphasis, half dB step size volume control, ATAPI channel mixing, selectable fast and slow digital interpolation filters followed by an oversampled multi-bit delta-sigma modulator that includes mismatch shaping technology that eliminates distortion due to capacitor mismatch. Following this stage is a multi-element switched capacitor stage and low pass filter with differential analog outputs.

The M9000 also has a proprietary DSD processor that allows for volume control and 50 kHz on-chip filtering without an intermediate decimation stage. It also offers an optional path for direct DSD conversion by directly using the multi-element switched capacitor array.

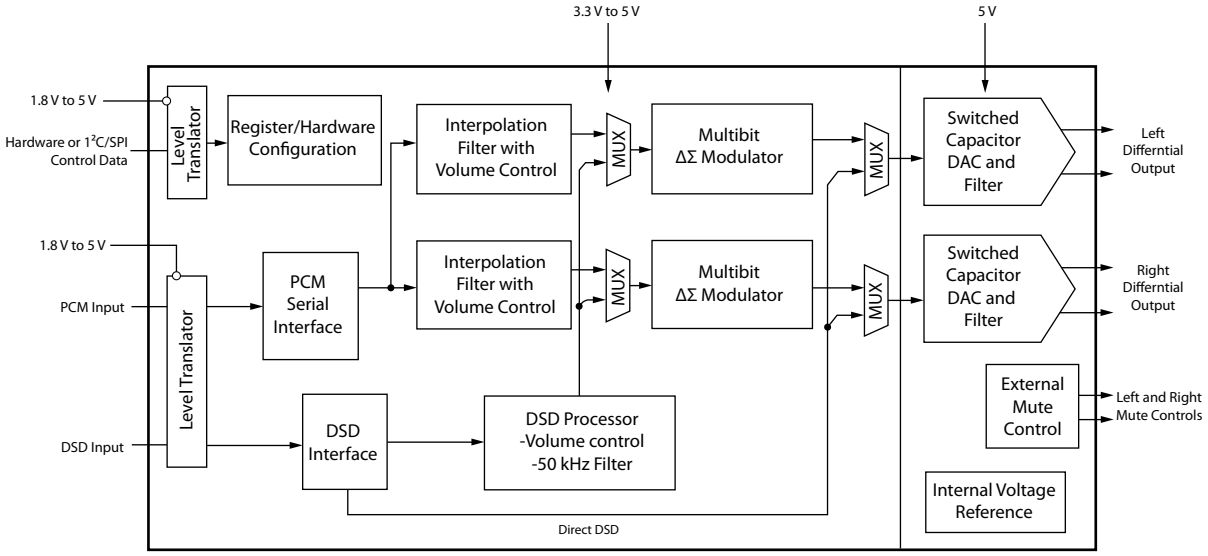


Figure 1. M9000 Block Diagram

Features

- Advanced Multibit Delta-Sigma Architecture
  - 120 dB Dynamic Range
  - -107 dB THD+N
  - Low Clock Jitter Sensitivity
  - Differential Analog Outputs
- PCM input
  - 102 dB of Stopband Attenuation
  - Supports Sample Rates up to 192 kHz
  - Accepts up to 24 bit Audio Data
  - Supports All Industry Standard Audio Interface Formats
  - Selectable Digital Filter Response
  - Volume Control with 1/2 dB Step Size and Soft Ramp
  - Flexible Channel Routing and Mixing
  - Selectable De-Emphasis
- Supports Stand-Alone or I²C/SPI™ Configuration

  Embedded Level Translators
  - 1.8 V to 5 V Serial Audio Input
  - 1.8 V to 5 V Control Data Input
- Direct Stream Digital (DSD)
  - Dedicated DSD Input Pins
  - On-Chip 50 kHz Filter to Meet Scarlet Book SACD Recommendations
  - Matched PCM and DSD Analog Output Levels
  - Non-Decimating Volume Control with 1/2 dB Step Size and Soft Ramp
  - DSD Mute Detection
  - Supports Phase-Modulated Inputs
  - Optional Direct DSD Path to On-Chip Switched Capacitor Filter

- Control Output for External Muting
  - Independent Left and Right Mute Controls
  - Supports Auto Detection of Mute Output Polarity
- Typical Applications
  - DVD Players
  - SACD Players
  - A/V Receivers
  - Professional Audio Products

Stand-Alone Mode Features

- Selectable Oversampling Modes
  - 32 kHz to 54 kHz Sampling Rates
  - 50 kHz to 108 kHz Sampling Rates
  - 100 kHz to 216 kHz Sampling Rates
- Selectable Serial Audio Interface Formats
  - Left-Justified, up to 24 bit
  - I^2S, up to 24 bit
  - Right-Justified 16 bit
  - Right-Justified 24 bit
- Auto Mute Output Polarity Detect
- Auto Mute on Static PCM Samples
- 44.1 kHz 50/15 µs De-Emphasis Available
- Soft Volume Ramp-up after Reset is Released

Control Port Mode Features

- Selectable Oversampling Modes
  - 32 kHz to 54 kHz Sampling Rates
  - 50 kHz to 108 kHz Sampling Rates
  - 100 kHz to 216 kHz Sampling Rates
- Selectable Serial Audio Interface Formats
  - Left-Justified, up to 24 bit
  - I^2S, up to 24 bit
  - Right-Justified 16 bit
  - Right-Justified 18 bit
  - Right-Justified 20 bit
  - Right-Justified 24 bit
- Direct Stream Digital Mode
- Selectable Auto or Manual Mute Polarity
- Selectable Interpolation Filters
- Selectable 32, 44.1, and 48 kHz De-Emphasis
- Configurable ATAPI Mixing Functions
- Configurable Volume and Muting Controls

2. Pin Information

2.1 Pinout Drawing

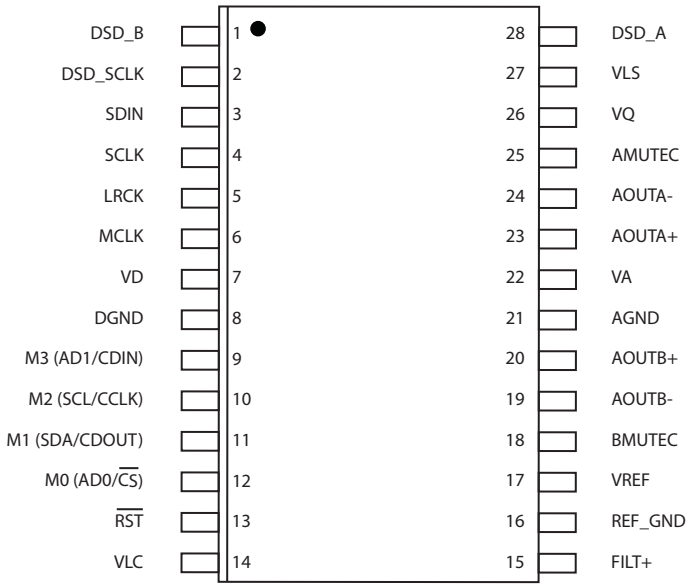


Figure 2. M9000 Pinout Drawing-TSSOP

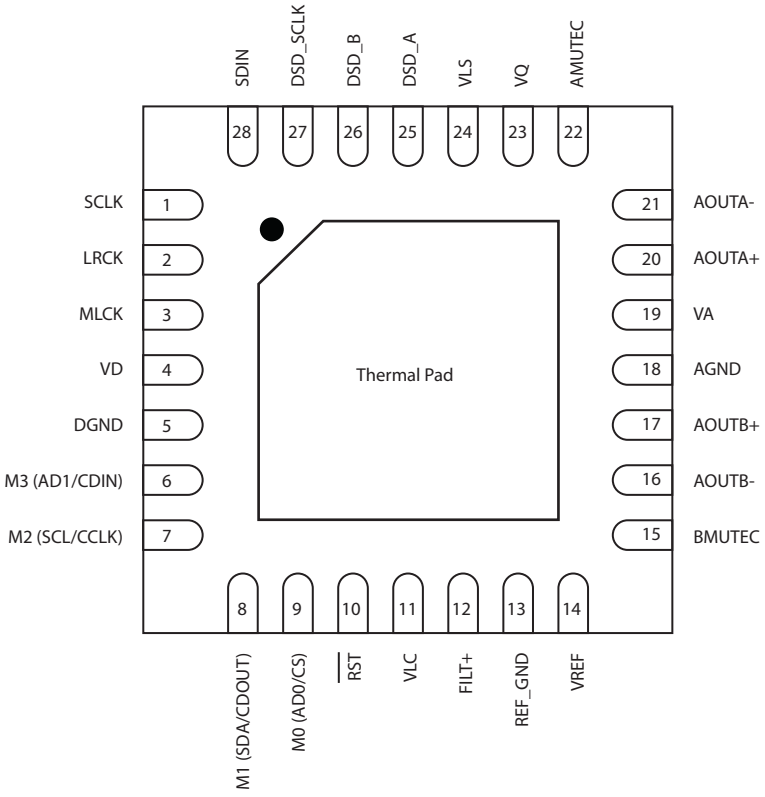


Figure 3. M9000 Pinout Drawing-QFN

2.2 Pin Description

Pin No.		Pin Name	Description
TSSOP	QFN		
28 1	25 26	DSD_A DSD_B	**Direct Stream Digital Input** *(Input)* - Input for Direct Stream Digital serial audio data.
2	27	DSD_SLCK	**DSD Serial Clock** *(Input)* - Serial clock for the Direct Stream Digital audio interface.
3	28	SDIN	**Serial Audio Data Input** *(Input)* - Input for two's complement serial audio data.
4	1	SCLK	**Serial Clock** *(Input)* - Serial clock for the serial audio interface.
5	2	LRCK	**Left Right Clock** *(Input)* - Determines which channel, Left or Right, is currently active on the serial audio data line.
6	3	MCLK	**Master Clock** *(Input)* - Clock source for the delta-sigma modulator and digital filters.
7	4	VD	**Digital Power** *(Input)* - Positive power for the digital section.
8	5	DGND	**Digital Ground** *(Input)* - Ground reference for the digital section.
13	10	$\overline{\text{RST}}$	**$\overline{\text{Reset}}$** *(Input)* - The device enters system reset when enabled.
14	11	VLC	**Control Port Power** *(Input)* - Positive power for Control Port I/O.
15	12	FILT+	**Positive Voltage Reference** *(Output)* - Positive reference voltage for the internal sampling circuits.
16	13	REF_GND	**Reference Ground** *(Input)* - Ground reference for the internal sampling circuits.
17	14	VREF	**Voltage Reference** *(Input)* - Positive voltage reference for internal sampling circuits.
18 25	15 22	BMUTEC AMUTEC	**Mute Control** *(Output)* - The Mute Control pin is active during power-up initialization, muting, power-down or if the master clock to left/right clock frequency ratio is incorrect. During reset, these outputs are set to a high impedance.
20 19	17 16	AOUTB+ AOUTB-	**Differential Right Channel Analog Output** *(Output)* - The full-scale differential analog output level is specified in the Analog Characteristics specification table.
21	18	AGND	**Analog Ground** *(Input)* - Ground reference for the analog section.
22	19	VA	**Analog Power** *(Input)* - Positive power for the analog section.
23 24	20 21	AOUTA+ AOUTA-	**Differential Left Channel Analog Output** *(Output)* - The full-scale differential analog output level is specified in the Analog Characteristics specification table.
26	23	VQ	**Quiescent Voltage** *(Output)* - Filter connection for internal quiescent voltage.
27	24	VLS	**Serial Audio Interface Power** *(Input)* - Positive power for serial audio interface I/O.
Stand-Alone Mode Definitions			
9 10 11 12	6 7 8 9	M3 M2 M1 M0	**Mode Selection** *(Input)* - Determines the operational mode of the device.
Control Port Mode			
9	6	AD1/CDIN	**Address Bit 1 (I^2C) / Control Data Input (SPI)** *(Input)* - AD1 is a chip address pin in I^2C mode; CDIN is the input data line for the Control Port interface in SPI mode.
10	7	SCL/CCLK	**Serial Control Port Clock** *(Input)* - Serial clock for the serial Control Port.
11	8	SDA/CDOUT	**Serial Control Data (I^2C) / Control Data Output (SPI)** *(Input/Output)* - SDA is a data I/O line in I^2C mode. CDOUT is the output data line for the Control Port interface in SPI mode.
12	9	AD0/$\overline{\text{CS}}$	**Address Bit 0 (I^2C) / Control Port Chip Select (SPI)** *(Input)* - AD0 is a chip address pin in I^2C mode; CS is the chip select signal for SPI format.
Recommended Connection for QFN package			
N/A	—	Thermal Pad	

3. Characteristics and Specifications

(Min/Max performance characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics are derived from measurements taken at T_A = 25°C, VA = 5.0 V, VD = 3.3 V.)

3.1 Absolute Maximum Ratings

(AGND = 0 V; all voltages with respect to ground.)

Characteristic		Symbol	Min	Max	Units
DC Power Supplies	Analog power	VA	-0.3	+6.0	V
	Voltage reference	VREF	-0.3	+6.0	
	Digital power	VD	-0.3	+6.0	
	Serial audio interface power	VLS	-0.3	+6.0	
	Control port interface power	VLC	-0.3	+6.0	
Input Current		Iin	-10	+10	mA
Digital Input Voltage	Serial audio interface	V_{IN-LS}	-0.3	V_{LS}+ 0.4	V
	Control port interface	V_{IN-LC}	-0.3	V_{LC}+ 0.4	
Ambient Operating Temperature (Power Applied)		T_A	-55	+125	°C
Storage Temperature		T_{stg}	-65	+150	

3.2 Recommended Operating Conditions

GND = 0 V, all voltages with respect to 0 V.

Characteristic		Symbol	Min	Typ	Max	Units
DC Power Supplies	Analog power	VA	4.75	5.0	5.25	V
	Voltage reference	VREF	4.75	5.0	5.25	
	Digital power	VD	3.14	3.3	5.25	
	Serial audio interface power	VLS	1.71	3.3	5.25	
	Control port interface power	VLC	1.71	3.3	5.25	
Specified Temperature Range	-CZ & -CZZ	T_A	-10		70	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

3.3 Analog Characteristics

(Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth is 10 Hz to 20 kHz; test load RL = 1 k□, CL = 10 pF.)

Parameter			Symbol	Min	Typ	Max	Units
Dynamic Performance - All PCM modes and DSD Processor mode							
Dynamic Range (Note 1)		24-bit A-Weighted		114	120	—	dB
		Unweighted		111	117	—	
		16-bit A-Weighted		—	97	—	
		(Note 2) unweighted		—	94	—	
Total Harmonic Distortion + Noise		(Note 1)		—	-107	-100	dB
	24-bit	0 dB		—	-97	—	
		-20 dB		—	-57	—	
		-60 dB	THD+N	—	-94	—	
	16-bit	0 dB		—	-74	—	
	(Note 2)	-20 dB		—	-34	—	
		-60 dB					
Idle Channel Noise / Signal-to-noise ratio				—	120	—	dB
Dynamic Performance - Direct DSD							
Dynamic Range (Note 3)		A-Weighted		111	117	—	dB
		unweighted		108	114	—	
Total Harmonic Distortion + Noise		(Note 3)		—	-104	-98	dB
	24-bit	0 dB	THD+N	—	-94	—	
		-20 dB		—	-54	—	
		-60 dB					
Dynamic Performance for All Modes							
Interchannel Isolation		(1 kHz)		—	110	—	dB
DC Accuracy							
Interchannel Gain Mismatch				—	0.1	—	dB
Gain Error				-7		7	%
Gain Drift				—	100	—	ppm/°C
Analog Input Characteristics and Specifications							
Full-scale Differential Input Voltage		PCM, DSD processor		132%•V_A	134%•V_A	136%•V_A	Vpp
		Direct DSD mode		94%•V_A	96%•V_A	98%•V_A	
Output Impedance			Z_{OUT}	—	118	—	Ω
Minimum AC-Load Resistance			R_L	—	1	—	kΩ
Maximum Load Capacitance			C_L	—	100	—	pF

Notes:
1. One LSB of triangular PDF dither is added to data.
2. Performance limited by 16-bit quantization noise.
3. DSD performance may be limited by the source recording. 0 dB-SACD = 50% modulation index.

3.4 Combined Interpolation & On-Chip Analog Filter Response

The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.)
(See note 9.)

Parameter		Fast Roll-Of			Unit
		Min	Typ	Max	
Combined Digital and On-Chip Analog Filter Response - Single-Speed Mode - 48 kHz (Note 5)					
Passband (Note 6)	to -0.01 dB corner to -3 dB corner	0 0	— —	0.454 0.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	—	+0.01	dB
Stopband		0.547	—	—	Fs
Stopband Attenuation	(Note 7)	102	—	—	dB
Group Delay		—	9.4/Fs	—	s
De-emphasis Error (Note 8) (Relative to 1 kHz)	Fs=32 kHz Fs=44.1 kHz Fs=48 kHz	— — —	— — —	±0.23 ±0.14 ±0.09	dB
Combined Digital and On-Chip Analog Filter Response - Double-Speed Mode - 96 kHz (Note 5)					
Passband (Note 6)	to -0.01 dB corner to -3 dB corner	0 0	— —	0.430 0.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	—	+0.01	dB
Stopband		0.583	—	—	Fs
Stopband Attenuation	(Note 7)	80	—	—	dB
Group Delay		—	4.7/Fs	—	s
Combined Digital and On-Chip Analog Filter Response - Quad-Speed Mode - 192 kHz (Note 5)					
Passband (Note 6)	to -0.01 dB corner to -3 dB corner	0 0	— —	0.105 0.490	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	—	+0.01	dB
Stopband		0.635	—	—	Fs
Stopband Attenuation	(Note 7)	90	—	—	dB
Group Delay		—	4.7/Fs	—	s

Parameter		Slow Roll-Off (Note 4)			Unit
		Min	Typ	Max	
Single-Speed Mode - 48 kHz (Note 5)					
Passband (Note 6)	to -0.01 dB corner to -3 dB corner	0 0	— —	0.417 0.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	—	+0.01	dB
Stopband		0.583	—	—	Fs
Stopband Attenuation	(Note 7)	64	—	—	dB
Group Delay		—	6.65/Fs	—	s
De-emphasis Error (Note 8) (Relative to 1 kHz)	Fs=32 kHz Fs=44.1 kHz Fs=48 kHz	— — —	— — —	±0.23 ±0.14 ±0.09	dB
Double-Speed Mode - 96 kHz (Note 5)					
Passband (Note 6)	to -0.01 dB corner to -3 dB corner	0 0	— —	0.296 0.499	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	—	+0.01	dB
Stopband		0.792	—	—	Fs
Stopband Attenuation	(Note 7)	70	—	—	dB
Group Delay		—	3.9/Fs	—	s
Quad-Speed Mode - 192 kHz (Note 5)					
Passband (Note 6)	to -0.01 dB corner to -3 dB corner	0 0	— —	0.104 0.481	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	—	+0.01	dB
Stopband		0.868	—	—	Fs
Stopband Attenuation	(Note 7)	75	—	—	dB
Group Delay		—	4.2/Fs	—	s

Notes:

4. Slow Roll-off interpolation filter is only available in Control Port mode.
5. Filter response is guaranteed by design.
6. Response is clock-dependent and will scale with Fs.
7. For Single-Speed Mode, the Measurement Bandwidth is from stopband to 3 Fs.
   For Double-Speed Mode, the Measurement Bandwidth is from stopband to 3 Fs.
   For Quad-Speed Mode, the Measurement Bandwidth is from stopband to 1.34 Fs.
8. De-emphasis is available only in Single-Speed Mode; Only 44.1 kHz De-emphasis is available in StandAlone mode.
9. Amplitude vs. Frequency plots of this data are available in the “Appendix” on page "11. Appendix" on page 43.

3.5 DSD Combined Digital & On-Chip Analog Filter Response

Parameter		Min	Typ	Max	Unit
DSD Processor Mode (Note 6)					
Passband (Note 6)	to -3 dB corner	0	—	50	kHz
Frequency Response 10 Hz to 20 kHz		-0.05	—	+0.05	dB
Roll-off		27	—	—	dB/Oct
Direct DSD Mode (Note 5)					
Passband (Note 6)	to -0.01 dB corner to -3 dB corner	0 0	— —	26.9 176.4	kHz
Frequency Response 10 Hz to 20 kHz		-0.1	—	+0.05	dB

3.6 Switching Characteristics-PCM

(Inputs: Logic 0 = GND, Logic 1 = VLS, C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Unit
Input Sample Rates	Single-Speed Mode Double-Speed Mode Quad-Speed Mode	Fs	30 50 100	—	54 108 216	kHz
MCLK Frequency		See Tables 1 & 2 (page 22) for compatible frequencies				
MCLK Duty Cycle			40	—	60	%
LRCK Duty Cycle			45	50	55	
SCLK Pulse Width Low		t_{sclkl}	20	—	—	ns
SCLK Pulse Width High		t_{sclkh}	20	—	—	
SCLK Period	Single-Speed Mode Double-Speed Mode Quad-Speed Mode	t_{sclkw}	1/(128)Fs 1/(64)Fs 1/(2)Fs	— — —	— — —	
SCLK rising to LRCK edge delay		t_{slrd}	20	—	—	
SCLK rising to LRCK		t_{slrs}	20	—	—	
SDATA valid to SCLK		t_{sdlrs}	22	—	—	
SCLK rising to SDATA hold time		t_{sdh}	20	—	—	

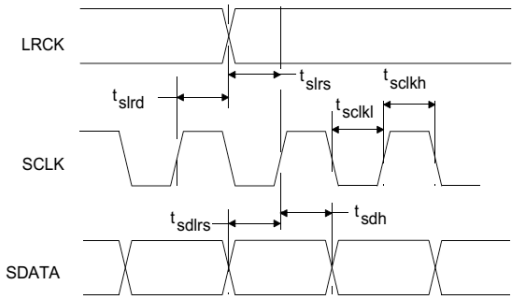


Figure 4. Serial Mode Input Timing

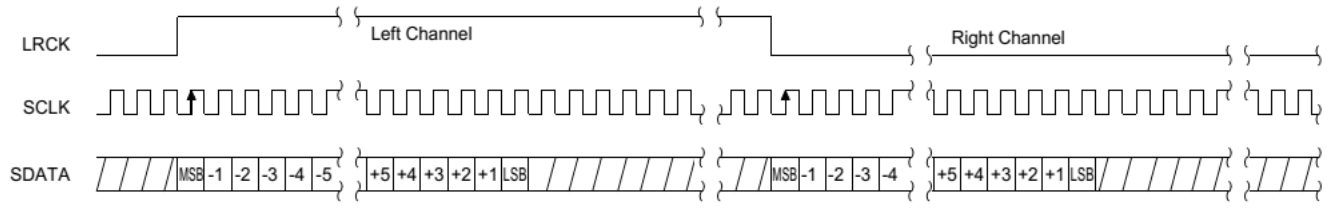


Figure 5. Format 0 - Left-Justified up to 24-bit Data

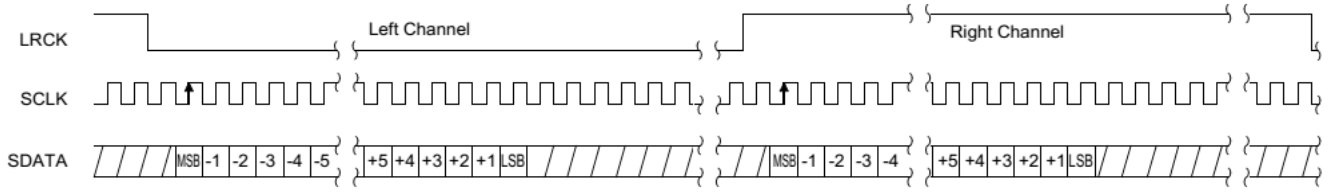


Figure 6. Format 1 - I^2S up to 24-bit Data

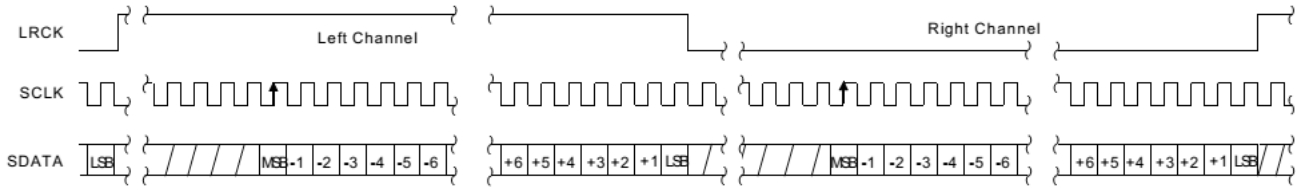


Figure 7. Format 2, Right-Justified 16-Bit Data.
Format 3, Right-Justified 24-Bit Data.
Format 4, Right-Justified 20-Bit Data. (Available in Control Port Mode only)
Format 5, Right-Justified 18-Bit Data. (Available in Control Port Mode only)

3.7 Switching Characteristics-DSD

(Logic 0 = AGND = DGND; Logic 1 = VLS Volts; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
MCLK Duty Cycle		40	—	60	%
DSD_SCLK Pulse Width Low	t_{sclkl}	160	—	—	ns
DSD_SCLK Pulse Width High	t_{sclkh}	160	—	—	
DSD_SCLK Frequency (64x Oversampled) (128x Oversampled)		1.024 2.048	— —	3.2 6.4	MHz
DSD_A / _B valid to DSD_SCLK rising setup time	t_{sdlrs}	20	—	—	ns
DSD_SCLK rising to DSD_A or DSD_B hold time	t_{sdh}	22	—	—	
DSD clock to data transition (Phase Modulation mode)	t_{dpm}	-20	—	20	

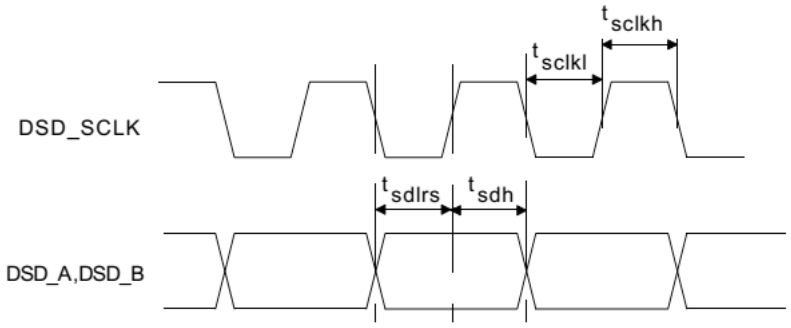


Figure 8. Direct Stream Digital - Serial Audio Input Timing

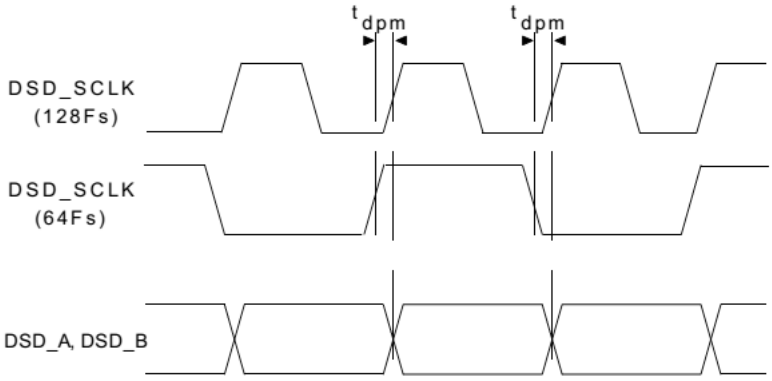


Figure 9. Direct Stream Digital - Serial Audio Input Timing for Phase Modulation Mode

3.8 Switching Characteristics- Control Port - I²C Format

(Inputs: Logic 0 = GND, Logic 1 = VLC, CL = 20 pF)

Parameter	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	—	100	kHz
$\overline{RST}$ Rising Edge to Start	t_{irs}	500		ns
Bus Free Time Between Transmissions	t_{buf}	4.7		µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0		
Clock Low time	t_{low}	4.7		
Clock High Time	t_{high}	4.0	—	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7		
SDA Hold Time from SCL Falling (Note 10)	t_{hdd}	0		
SDA Setup time to SCL Rising	t_{sud}	250		ns
Rise Time of SCL and SDA	t_{rc},t_{rd}	—	1	µs
Fall Time of SCL and SDA	t_{fc},t_{fd}	—	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs
Acknowledge Delay from SCL Falling	t_{ack}	300	1000	ns

10. Data must be held for sufficient time to bridge the transition time, tfc, of SCL.

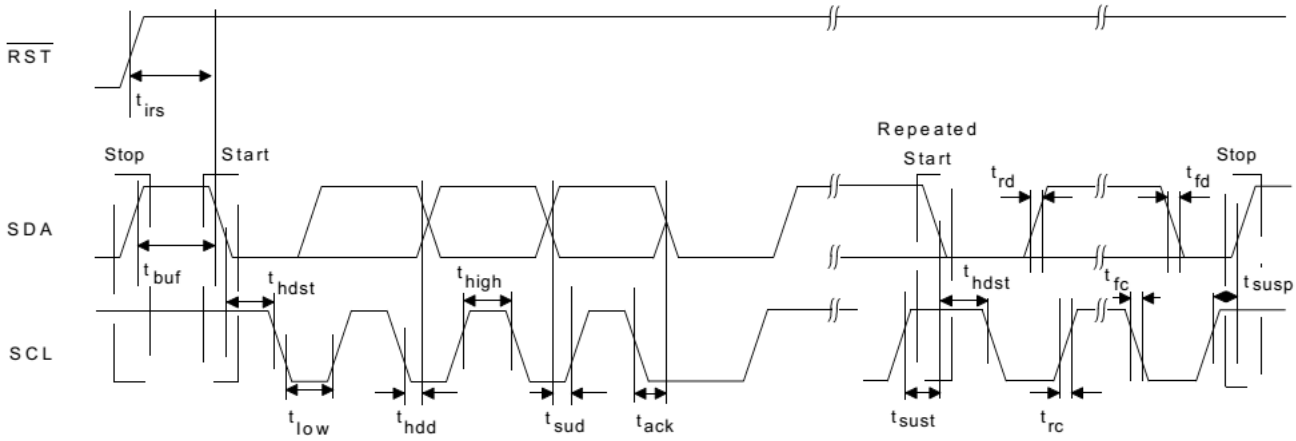


Figure 10. Control Port Timing - I²C Format

3.9 Switching Characteristics- Control Port - SPI™ Format

(Inputs: Logic 0 = GND, Logic 1 = VLC, C_L = 20 pF)

Parameter		Symbol	Min	Max	Units
CCLK Clock Frequency		f_{sck}	0	6	MHz
$\overline{RST}$ Rising Edge to $\overline{CS}$ Falling		t_{srs}	500		ns
CCLK Edge to $\overline{CS}$ Falling	(Note 11)	t_{spi}	500		
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0		µs
$\overline{CS}$ Falling to CCLK Edge		t_{css}	20	—	ns
CCLK Low Time		t_{scl}	66		
CCLK High Time		t_{sch}	66		
CDIN to CCLK Rising Setup Time		t_{dsu}	40		
CCLK Rising to DATA Hold Time	(Note 12)	t_{dh}	15		
Rise Time of CCLK and CDIN	(Note 13)	t_r2	—	100	
Fall Time of CCLK and CDIN	(Note 13)	t_f2		100	
Transition time from CCLK to CDOUT valid	(Note 14)	t_{scdov}		40	
Time from CS rising to CDOUT high-Z	(Note 15)	t_{cscdo}		20	

11. t_{spi} only needed before first falling edge of CS after RST rising edge. tspi = 0 at all other times.
12. Data must be held for sufficient time to bridge the transition time of CCLK.
13. For F_{SCK} < 1 MHz.
14. CDOUT should *not* be sampled during this time period.
15. This time is by design and not tested.

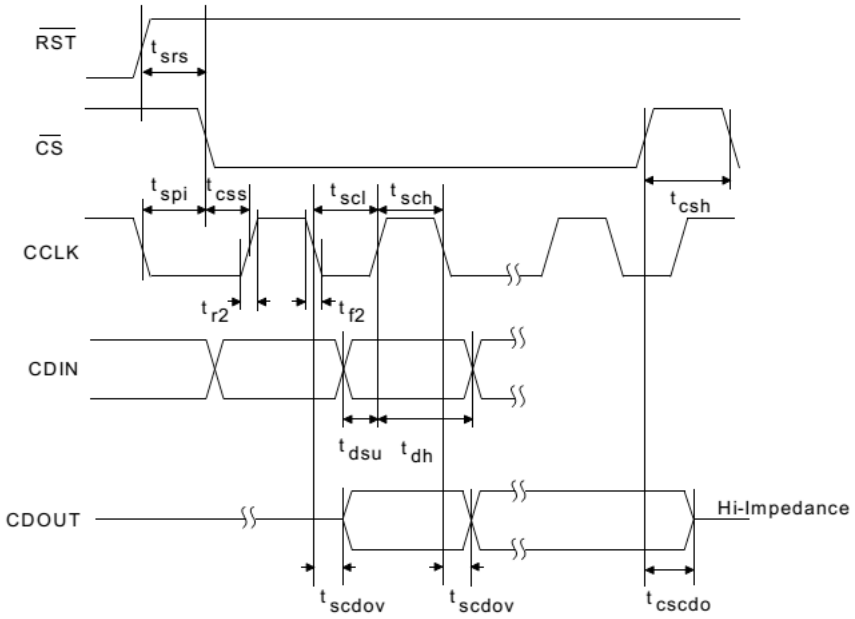


Figure 11. Control Port Timing - SPI™ Format(Read/Write)

3.10 Dc Electrical Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Normal Operation *(Note 16)*						
Power Supply Current	VA = 5 V(NOTE17) VREF = 5V VD = 5V VD = 3.3V Interface current (Note 18)	I_A I_{REF} I_D I_D I_{LC} I_{LS}	—	25 1.5 25 18 2 80	28 2 38 27 — —	mA µA
Power Dissipation	VA = 5V,VD = 5V VA = 5V,VD = 3.3V		—	258 192	340 240	mW
Power —Down Mode *(Note 19)*						
Power Supply Current		I_{PD}	—	200	—	µA
Power Dissipation	VA = 5V,VD = 5V VA = 5V,VD = 3.3V		—	1 1	—	mW
All Modes of Operation						
Power Supply Rejection Ratio (Note 20)	(1 kHz) (60 Hz)	P_{SRR}	—	60 40	—	dB
Common Mode Voltage		V_Q	—	0.5•VA	—	V
Max Current draw from VQ		I_{QMAX}	—	1	—	µA
FILT+ Nominal Voltage			—	0.93•VA	—	V
Maximum MUTEC Drive Current	(Note 21)		—	3	—	mA
MUTEC High —Level Output Voltage		V_{OH}	—	V_A	—	V
MUTEC Low —Level Output Voltage		V_{OL}	—	0	—	

16. Normal operation is defined as RST pin = High with a 997 Hz, 0 dBFS input sampled at the highest Fs for each speed mode, and open outputs, unless otherwise specified.
17. I_A measured with no loading on the AMUTEC and BMUTEC pins.
18. I_{LC} measured with no external loading on pin 11 (SDA).
19. Power-Down mode is defined as RST pin = Low with all clock and data lines held static.
20. Valid with the recommended capacitor values on FILT+ and VQ as shown in the "Typical Connection Diagram" on page 17.
21. This current is sourced/sinked directly from the VA supply

3.11 Digital Interface Specifications

Parameter			Symbol	Min.	Typ.	Max.	Unit
Input Leakage Current			I_{IN}	-10	—	10	mA
Input Capacitance				—	8	—	pF
High-Level Input Voltage	Serial I/O		V_{IH}	70%	—	—	V_{LS}
		Control I/O	V_{IH}	70%			V_{LC}
Low-Level Input Voltage	Serial I/O		V_{IL}	—	—	30%	V_{LS}
		Control I/O	V_{IL}			30%	V_{LC}
High-Level Output Voltage (I_{OH} = -1.2 mA) Control I/O			V_{OH}	80%	—	—	
Low-Level Output Voltage (I_{OL} = 1.2 mA) Control I/O			V_{OL}	—	—	20%	
MUTEC auto detect input high voltage				70%	—	—	V_A
MUTEC auto detect input low voltage				—	—	30%	

4. Typical Connection Diagram

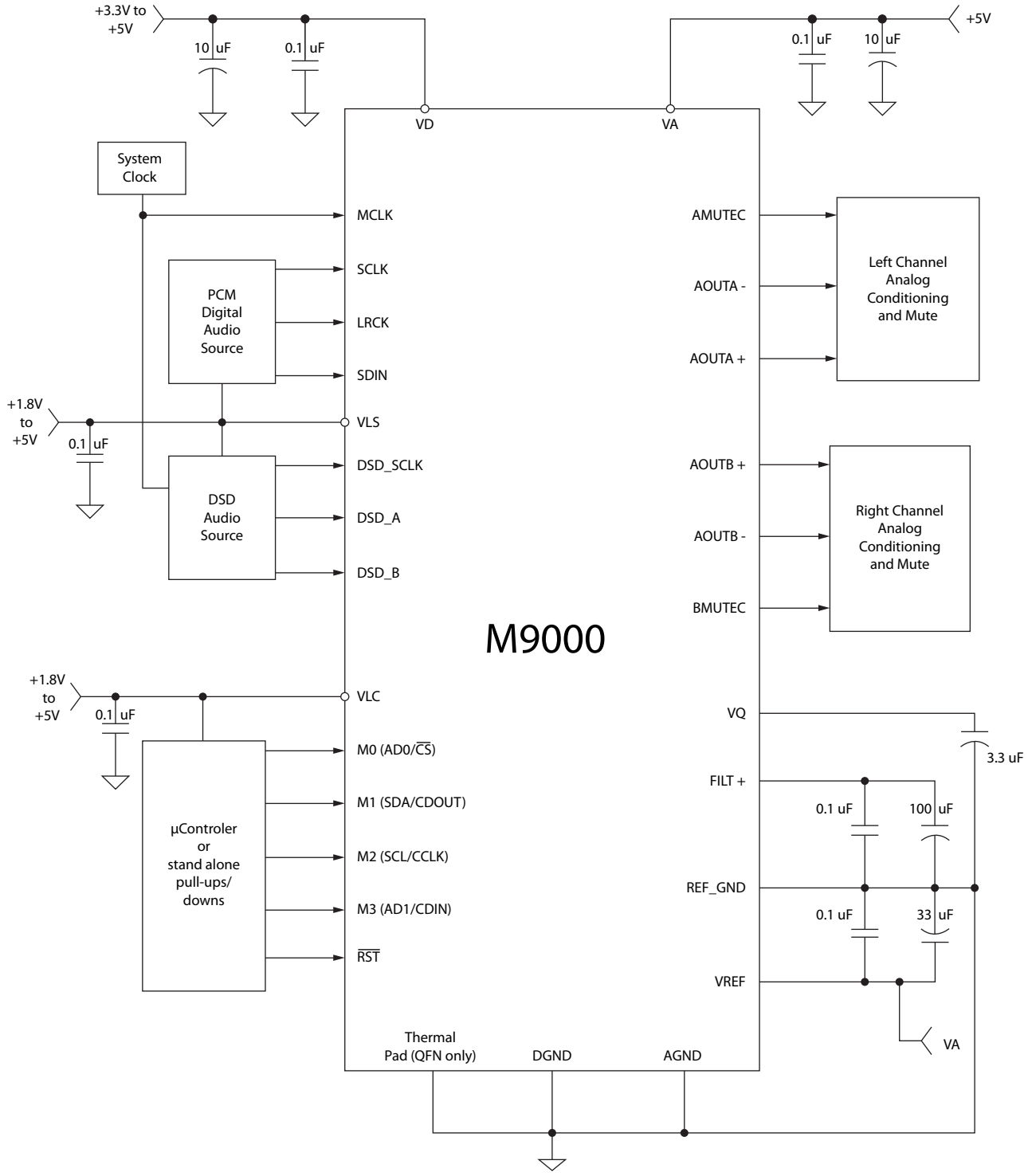


Figure 12. Typical Connection Diagram

5. Applications

5.1 Grounding and Power Supply Decoupling

As with any high resolution converter, the M9000 requires careful attention to power supply and grounding arrangements to optimize performance. The Typical Connection Diagram shows the recommended power arrangement with VA, VD, VLS and VLC connected to clean supplies. Decoupling capacitors should be located as close to the device package as possible. If desired, all supply pins may be connected to the same supply, but the recommended decoupling capacitors should still be placed on each supply pin. The AGND and DGND pins should be tied together with solid ground plane fill underneath the converter extending out to the GND side of the decoupling caps for VA, VD, VREF, and FILT+. This recommended layout can be seen in the evaluation board and datasheet. For the QFN package, the thermal pad should also be tied to ground for thermal dissipation.

5.2 Analog Output and Filtering

The Cirrus Logic application note "Design Notes for a 2-Pole Filter with Differential Input" discusses the second-order Butterworth filter and differential to single-ended converter topology that was implemented on the M9000 evaluation board, as seen in **Figure 13.**

The M9000 does not include phase or amplitude compensation for an external filter. Therefore, the DAC system phase and amplitude response is dependent on the external analog circuitry.

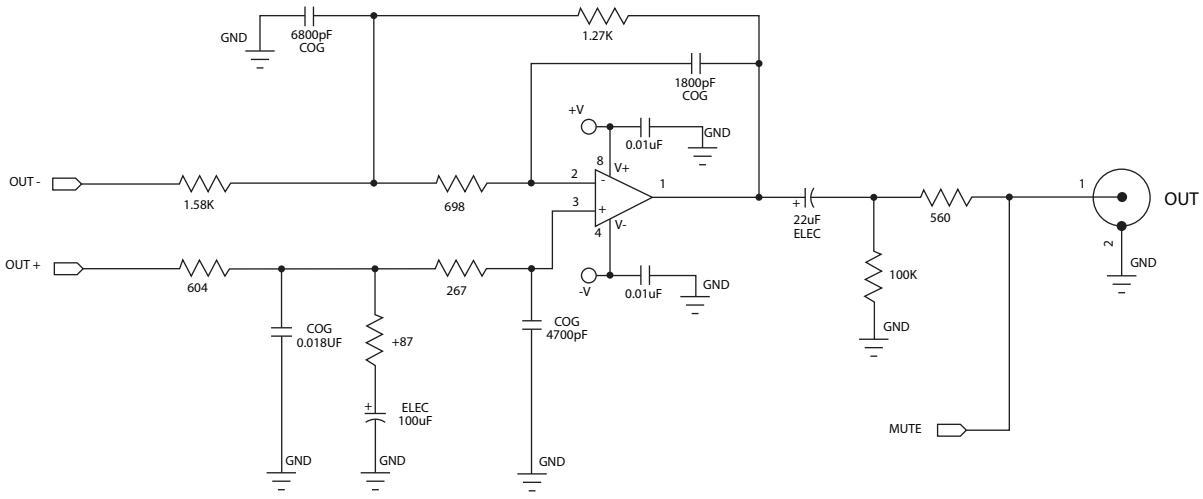


Figure 13. Recommended Output Filter

5.3 The MUTEC Outputs

The AMUTEC and BMUTEC pins have an auto-polarity detect feature. The MUTEC output pins are high impedance at the time of reset. The external mute circuitry needs to be self-biased into an active state in order to be muted during reset. Upon release of reset, the M9000 detects the status of the MUTEC pins (high or low) and then selects that state as the polarity to drive when the mutes become active. The externalbias voltage level that the MUTEC pins see at the time of release of reset must meet the "MUTEC auto detect input high/low voltage" specifications as outlined in the Digital Characteristics in Section 3.

Figure 14. shows a single example of both an active-high and an active-low mute drive circuit. In these designs, the pull-up and pull-down resistors have been specifically chosen to meet the input high/low threshold when used with the MMUN2111 and MMUN2211 internal bias resistances of 10 kΩ .

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit.

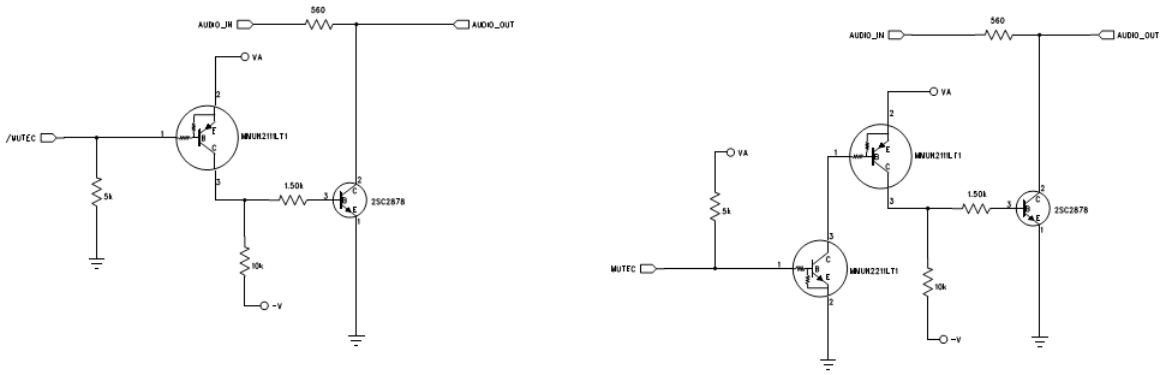


Figure 14. Recommended Mute Circuitry

5.4 Oversampling Modes

The M9000 operates in one of three oversampling modes based on the input sample rate. Single-Speed mode supports input sample rates up to 50 kHz and uses a 128x oversampling ratio. Double-Speed mode supports input sample rates up to 100 kHz and uses an oversampling ratio of 64x. Quad-Speed mode supports input sample rates up to 200 kHz and uses an oversampling ratio of 32x.

5.5 Master and Serial Clock Ratios

The required MCLK-to-LRCK ratio and suggested SCLK-to-LRCK ratio are outlined in **Table 1.** MCLK can be at any phase in regards to LRCK and SCLK. SCLK, LRCK and SDATA must meet the phase and timing relationships outlined in Section 2. Some common MCLK frequencies have been outlined in **Table 2**

	MCLK/LRCK	SCLK/LRCK	LRCK
Single-Speed	256, 384,5 12, 768*,1024*, 1152*	32, 48, 64, 96, 128	Fs
Double-Speed	128, 192, 256, 384, 512*	32, 48, 64	Fs
Quad-Speed	64	32 (16 bits only)	Fs
	96	32,48	Fs
	128, 256*	32, 64	Fs
	192	32, 48, 64, 96	Fs

**These modes are only available in Control Port mode by setting the appropriate MCLKDIV bit*

Table 1. Clock Ratios

Mode (sample-rate range	Sample Rate (kHz)	MCLK (MHz)					
					MCLKDIV2		MCLKDIV3
MCLK Ratio		**256x**	**384x**	**512x**	**768x**	**1024x**	**1152x**
Single-Speed (32 to 50 kHz)	32	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640
	44.1	11.2896	16.9344	22.5792	33.8688	45.1584	—
	48	12.2880	18.4320	24.5760	36.8640	49.1520	—
MCLK Ratio		**128x**	**192x**	**256x**	**384x**	**512x**	—
Double-Speed (50 to 100 kHz)	64	8.1920	12.2880	16.3840	24.5760	32.7680	—
	88.2	11.2896	16.9344	22.5792	33.8688	45.1584	—
	96	12.2880	18.4320	24.5760	36.8640	49.1520	—
MCLK Ratio		**64x***	**96x**	**128x**	**192x**	**256x**	—
Quad-Speed (100 to 200 kHz)	176.4	11.2896*	16.9344	22.5792	33.8688	45.1584	—
	192	12.2880	18.4320	24.5760	36.8640	49.1520	—
These modes are only available in Control Port mode by setting the appropriate MCLKDIV bit.							

*This MCLK ratio limits the audio word lenght to 16 bits; see Table 1 on page 21

Table 2. Common Clock Frequencies

5.6 Stand-Alone Mode Settings

In Stand-Alone mode (also referred to as "Hardware mode"), the device is configured using the M0 through M3 pins. These pins must be connected to either the VLC supply or ground. The Interface format is set by pins M0 and M1. The sample rate range/oversampling mode (Single/Double/Quad-Speed mode) and deemphasis are set by pins M2 and M3. The settings can be found in **Table 3** and **Table 4**.

M1	M0	Description	Format	Figure
0	0	Left-Justified, up to 24-bit data	0	4
0	1	I^2S, up to 24-bit data	1	5
1	0	Right-Justified, up to 16-bit data	2	6
1	1	Right-Justified, up to 24-bit data	3	6

Table 3. Digital Interface Format, Stand-Alone Mode Options

M1	M0	Description
0	0	Single-Speed without De-Emphasis (32 to 50 kHz sample rates)
0	1	Single-Speed with 44.1 kHz De-Emphasis; see Figure 18 on page page 27
1	0	Double-Speed (50 to 100 kHz sample rates)
1	1	Quad-Speed (100 to 200 kHz sample rates)

Table 4. Mode Selection, Stand-Alone Mode Options

The following features are always enabled in Stand-Alone mode: Auto-mute on zero data, Auto MUTEC polarity detect, ramp volume from mute to 0dB by 1/8th dB steps every LRCK (soft ramp) after reset or clock mode change, and the fast roll-off interpolation filter is used.

The following features are not available in Stand-Alone mode: DSD mode, Right-Justified 20- and 18-bit serial audio interfaces, MCLK divide-by-2 and MCLK divide-by-3 (allows 1024 and 1152 clock ratios), slow roll off interpolation filter, volume control, ATAPI mixing, 48 kHz and 32 kHz de-emphasis, and all other features enabled by registers that are not mentioned above.

5.6.1 Recommended Power-Up Sequence (Stand-Alone Mode)

1. Hold $\overline{RST}$ low until the power supply, master, and left/right clocks are stable. In this state, the Control Port is reset to its default settings.
2. Bring $\overline{RST}$ high. The device will remain in a low power state and will initiate the Stand-Alone powerup sequence following approximately 2^{18} MCLK cycles.

5.7 Control Port Mode

5.7.1 Recommended Power-Up Sequence (Control Port Mode)

1. Hold $\overline{\text{RST}}$ low until the power supply, master, and left/right clocks are stable. In this state, the Control Port is reset to its default settings.
2. Bring $\overline{\text{RST}}$ high. Set the CPEN bit (Reg. 8h) prior to the completion of the Stand-Alone power-up sequence (approximately 218 MCLK cycles). Setting this bit halts the Stand-Alone power-up sequence and initializes the Control Port to its default settings. The desired register settings can be loaded while keeping the PDN bit (Reg. 8h) set to 1.
3. Clear the PDN bit to initiate the power-up sequence.

If the CPEN bit is not written within the allotted time, the device will start-up in stand-alone mode and begin converting data according to the current state of the M0 to M3 pins. Since these pins are also the control port pins, an undesired mode may be entered. For this reason, if the CPEN bit is not set before the allotted time elapses, the SDIN line must be kept at static 0 (not dithered) until the device is properly configured. This will keep the device from converting data improperly.

5.7.2 Sample Rate Range/Oversampling Mode (Control Port Mode)

Sample rate mode selection is determined by the FM bits (Reg. 02h).

5.7.3 Serial Audio Interface Formats (Control Port Mode)

The desired serial audio interface format is selected using the DIF2:0 bits (Reg. 02h).

5.7.4 MUTEC Pins (Control Port Mode)

The auto-mute polarity feature (mentioned in Section 5.3) is defeatable. The MUTEP1:0 bits in register 04h give the option to override the mute polarity which was auto detected at startup (see the Register Description section for more details).

5.7.5 Interpolation Filter (Control Port Mode)

To accommodate the increasingly complex requirements of digital audio systems, the M9000 incorporates selectable interpolation filters. A fast and a slow roll-off filter are available in each of Single-, Double-, and Quad-Speed modes. These filters have been designed to accommodate a variety of musical tastes and styles. The FILT_SEL bit (Reg. 07h) is used to select which filter is used (see the Register Description section for more details).

Filter specifications can be found in Section 2, and filter response plots can be found in **Figure 23** to **Figure 46** in the “Appendix” on **page "11. Appendix" on page 43**.

5.7.6 Direct Stream Digital (DSD) Mode (Control Port Mode)

In Control Port mode, the FM bits (Reg. 02h) are used to configure the device for DSD mode. The DIF bits (Reg 02h) then control the expected DSD rate and MCLK ratio.

The DSD_SRC bit (Reg. 02h) selects the input pins for DSD clocks and data. During DSD operation, the PCM-related pins should either be tied low or remain active with clocks. When the DSD related pins are not being used, they should either be tied low or remain active with clocks.

The DIR_DSD bit (Reg 07h) selects between two proprietary methods for DSD-to-analog conversion. The first method uses a decimation-free DSD processing technique that allows for features such as matched PCM level output, DSD volume control, and 50 kHz on-chip filter. The second method sends the DSD data directly to the on-chip switched-capacitor filter for conversion (without the above mentioned features).

The DSD_PM_EN bit (Reg. 09h) selects Phase Modulation (data plus data inverted) as the style of data input. In this mode, the DSD_PM_mode bit selects whether a 128Fs or 64x clock is used for phase modulated 64x data (see Figure 14). Use of phase modulation mode may not directly affect the performance of the M9000, but may lower the sensitivity to board-level routing of the DSD data signals.

The M9000 can detect errors in the DSD data that do not comply to the SACD specification. The STATIC_DSD and INVALID_DSD bits (Reg. 09h) allow the M9000 to alter the incoming invalid DSD data. Depending on the error, the data may either be attenuated or replaced with a muted DSD signal (the MUTEC pins would set according to the DAMUTE bit (Reg. 04h)).

More information for any of these register bits can be found in the Register Description section.

The DSD input structure and analog outputs are designed to handle a nominal 0 dB-SACD (50% modulation index) at full rated performance. Signals of +3 dB-SACD may be applied for brief periods of time; however, performance at these levels is not guaranteed. If sustained +3 dB-SACD levels are required, the digital volume control should be set to -3.0 dB. This same volume control register affects PCM output levels. There is no need to change the volume control setting between PCM and DSD in order to have the 0 dB output levels match (both 0 dBFS and 0 dB-SACD will output at -3 dB in this case).

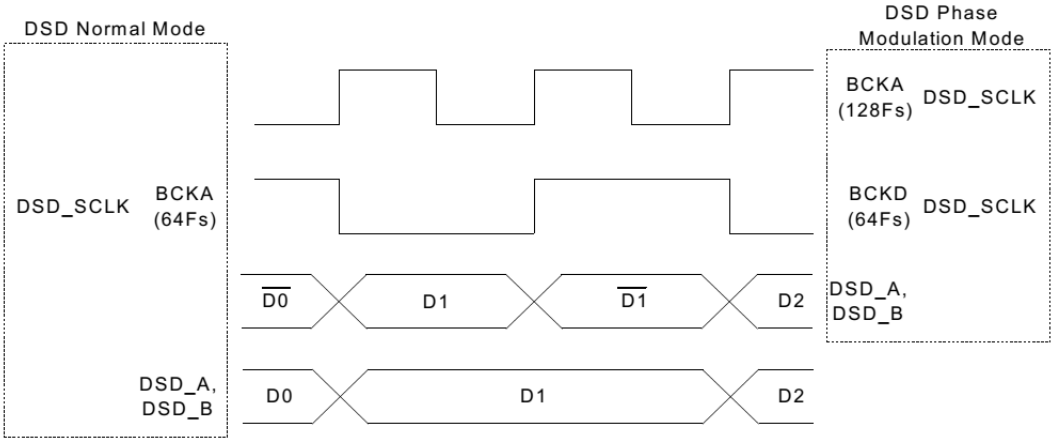


Figure 15. DSD Phase Modulation Mode Diagram

6. Control Port Interface

The Control Port is used to load all the internal settings. The operation of the Control Port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the Control Port pins should remain static if no operation is required.

6.1 Memory Address Pointer (MAP)

6.1.1 Memory Address Pointer (MAP) Register Detail

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	MAP3	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

6.1.2 INCR (Auto Map Increment Enable)

Default = '0'

0 - Disabled, the MAP will stay constant for successive writes

1 - Enabled, the MAP will auto increment after each byte is written, allowing block reads or writes of successive registers

6.1.3 MAP3-0 (Memory Address Pointer)

Default = '0000'

6.2 Enabling the Control Port

On the M9000, the Control Port pins are shared with Stand-Alone configuration pins. To enable the Control Port, the user must set the CPEN bit. This is done by performing an I^2C or SPI write. Once the Control Port is enabled, these pins are dedicated to Control Port functionality.

To prevent audible artifacts, the CPEN bit (see Section 7) should be set prior to the completion of the StandAlone power-up sequence, approximately 218 MCLK cycles. Setting this bit halts the stand-alone power-up sequence and initializes the Control Port to its default settings. Note, the CPEN bit can be set any time after $\overline{RST}$ goes high; however, setting this bit after the stand-alone power-up sequence has completed can cause audible artifacts.

6.3 Format Selection

The Control Port has two formats: SPI and I^2C, with the M9000 operating as a slave device.

If I^2C operation is desired, AD0/$\overline{CS}$ should be tied to VLC or GND. If the M9000 ever detects a high-to-low transition on AD0/$\overline{CS}$ after power-up, SPI format will automatically be selected

6.4 I^2C Format

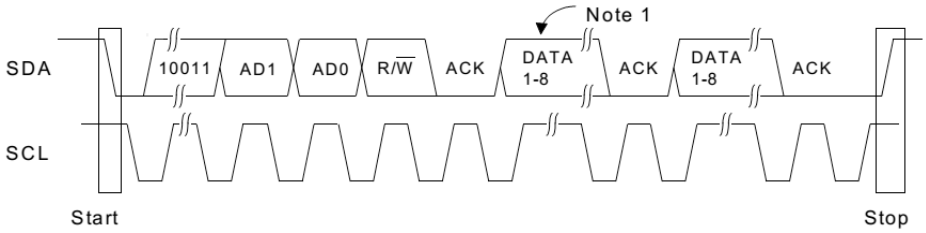
In I^2C Format, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL, with a clock-to-data relationship as shown in **Figure 16.** The receiving device should send an acknowledge (ACK) after each byte received. There is no $\overline{CS}$ pin. Pins AD0 and AD1 form the partial chip address and should be tied to VLC or GND as required. The upper five bits of the 7-bit address field must be 10011.

6.4.1 Writing in I^2C Format

To communicate with the M9000, initiate a START condition of the bus (see **Figure 16**). Next, send the chip address. The eighth bit of the address byte is the R/W bit (low for a write). The next byte is the Memory Address Pointer, MAP, which selects the register to be read or written. The MAP is then followed by the data to be written. To write multiple registers, continue providing a clock and data, waiting for the M9000 to acknowledge between each byte. To end the transaction, send a STOP condition.

6.4.2 Reading in I²C Format

To communicate with the M9000, initiate a START condition of the bus (see **Figure 16**). Next, send the chip address. The eighth bit of the address byte is the R/$\overline{W}$ bit (high for a read). The contents of the register pointed to by the MAP will be output after the chip address. To read multiple registers, continue providing a clock and issue an ACK after each byte. To end the transaction, send a STOP condition.



Note: If operation is a write, this byte contains the Memory Address Pointer, MAP.

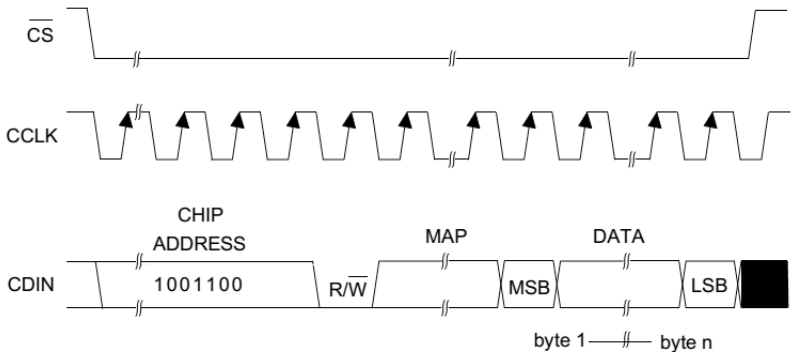
Figure 16. Control Port Timing, I²C Format

6.5 SPI Format

In SPI format, $\overline{CS}$ is the M9000 chip select signal; CCLK is the Control Port bit clock; CDIN is the input data line from the microcontroller; CDOUT is the output data line and the chip address is 1001100. $\overline{CS}$, CCLK, and CDIN are all inputs, and data is clocked in on the rising edge of CCLK. CDOUT is an output and is high-impedance when not actively outputting data.

6.5.1 Writing in SPI

Figure 17 shows the operation of the Control Port in SPI format. To write to a register, bring $\overline{CS}$ low. The first seven bits on CDIN form the chip address and must be 1001100. The eighth bit is a read/write indicator (R/$\overline{W}$), which must be low to write. The next eight bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next eight bits are the data that will be placed into register designated by the MAP. To write multiple registers, keep $\overline{CS}$ low and continue providing clocks on CCLK. End the read transaction by setting $\overline{CS}$ high.



MAP = Memory Address Pointer

Figure 17. Control Port Timing, SPI Format (Write)

6.5.2 Reading in SPI

Figure 18 shows the operation of the Control Port in SPI format. To read to a register, bring $\overline{CS}$ low. The first seven bits on CDIN form the chip address and must be 1001100. The eighth bit is a read/write control (R/$\overline{W}$), which must be high to read. The CDOUT line will then output the data from the register designated by the MAP. To read multiple registers, keep $\overline{CS}$ low and continue providing clocks on CCLK. End the read transaction by setting $\overline{CS}$ high. The CDOUT line will go to a high-impedance state once $\overline{CS}$ goes high.

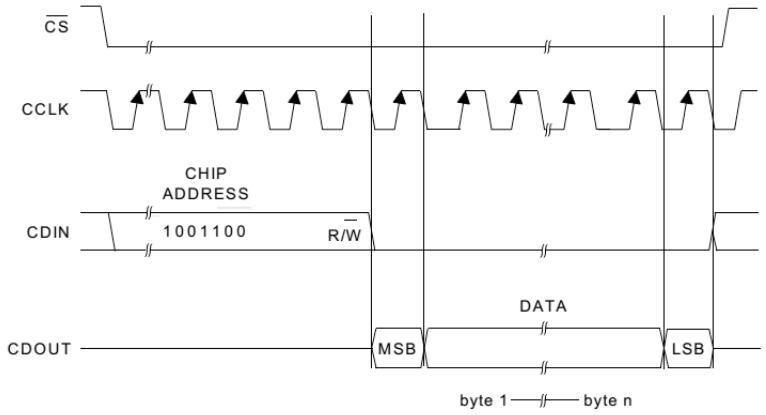


Figure 18. Control Port Timing, SPI Format (Read)

7. Register Quick Reference

Addr	Function	7	6	5	4	3	2	1	0
1h	Chip ID	PART4	PART3	PART2	PART1	PART0	REV2	REV1	REV0
	default	0	1	1	1	0	-	-	-
2h	Mode Control	DSD_SRC	DIF2	DIF1	DIF0	DEM1	DEM0	FM1	FM0
	default	0	0	0	0	0	0	0	0
3h	Volume, Mixing, and Inversion Control	VOLB=A	INVERTA	INVERTB	ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0
	default	0	0	0	0	1	0	0	1
4h	Mute Control	PAMUTE	DAMUTE	MUTEC A=B	MUTE_A	MUTE_B	Reserved	MUTEP1	MUTEP0
	default	1	1	0	0	0	0	0	0
5h	Channel A Volume Control	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
	default	0	0	0	0	0	0	0	0
6h	Channel B Volume Control	VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
	default	0	0	0	0	0	0	0	0
7h	Ramp and Filter Control	SZC1	SZC0	RMP_UP	RMP_DN	Reserved	FILT_SEL	Reserved	DIR_DSD
	default	1	0	1	1	0	0	0	0
8h	Misc. Control	PDN	CPEN	FREEZE	MCLKDIV2	MCLKDIV3	Reserved	Reserved	Reserved
	default	1	0	0	0	0	0	0	0
9h	Misc. Control 2	Reserved	Reserved	Reserved	Reserved	STATIC_ DSD	INVALID_ DSD	DSD_PM_ MODE	DSD_PM_ EN
	default	0	0	0	0	1	0	0	0

8. Register Description

** All register access is R/W unless specified otherwise**

8.1 Chip ID - Register 01h

7	6	5	4	3	2	1	0
PART4	PART3	PART2	PART1	PART0	REV2	REV1	REV0
0	1	1	1	0	-	-	-

Function:

This register is Read-Only. Bits 7 through 3 are the part number ID, which is 01110b (14h), and the remaining Bits (2 through 0) are for the chip revision (Rev. A = 000, Rev. B = 001, ...)

8.2 Mode Control 1 - Register 02h

7	6	5	4	3	2	1	0
DSD_SRC	DIF2	DIF2	DIF0	DEM1	DEM0	FM1	FM0
0	0	0	0	0	0	0	0

8.2.1 DSD Input Source Select (DSD_SRC) BIT 7

Function:

When set to 0 (default), the dedicated DSD pins will be the active DSD inputs.

When set to 1, the source for DSD inputs will be as follows:

DSDA input on SDATA pin
DSDB input on LRCK pin
DSD_SCLK input on SCLK pin

The dedicated DSD pins must be tied low while not in use.

8.2.2 Digital Interface Format (DIF2:0) BITs 6-4

Function:

These bits select the interface format for the serial audio input. The Functional Mode bits determine whether PCM or DSD mode is selected.

PCM Mode: The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format, and the options are detailed in **Figure 4** through **Figure 6**.

DIF2	DIF1	DIF0	Description	Format	Figure
0	**0**	**0**	**Left-Justified, up to 24-bit data**	**0 (Default)**	**4**
0	0	1	I²S, up to 24-bit data	1	5
0	1	0	Right-Justified, 16-bit data	2	6
0	1	1	Right-Justified, 24-bit data	3	6
1	0	0	Right-Justified, 20-bit data	4	6
1	0	1	Right-Justified, 18-bit data	5	6
1	1	0	Reserved		
1	1	1	Reserved		

Table 5. Digital Interface Formats - PCM Mode

DSD Mode: The relationship between the oversampling ratio of the DSD audio data and the required Master Clock to DSD data rate is defined by the Digital Interface Format pins.

DIF2	DIF1	DIF0	Description
0	**0**	**0**	**64x oversampled DSD data with a 4x MCLK to DSD data rate (Default)**
0	0	1	64x oversampled DSD data with a 6x MCLK to DSD data rate
0	1	0	64x oversampled DSD data with a 8x MCLK to DSD data rate
0	1	1	64x oversampled DSD data with a 12x MCLK to DSD data rate
1	0	0	128x oversampled DSD data with a 2x MCLK to DSD data rate
1	0	1	128x oversampled DSD data with a 3x MCLK to DSD data rate
1	1	0	128x oversampled DSD data with a 4x MCLK to DSD data rate
1	1	1	128x oversampled DSD data with a 6x MCLK to DSD data rate

Table 6. Digital Interface Formats - DSD Mode

8.2.3 De-Emphasis Control (DEM1:0) BITs 3-2

Default = 0
00 - No De-emphasis
01 - 44.1 kHz De-emphasis
10 - 48 kHz De-emphasis
11 - 32 kHz De-emphasis

Function:

Selects the appropriate digital filter to maintain the standard 15µS/50µS digital de-emphasis filter response at 32, 44.1 or 48 kHz sample rates. (see **Figure 19**)

Notes: De-emphasis is only available in Single-Speed Mode

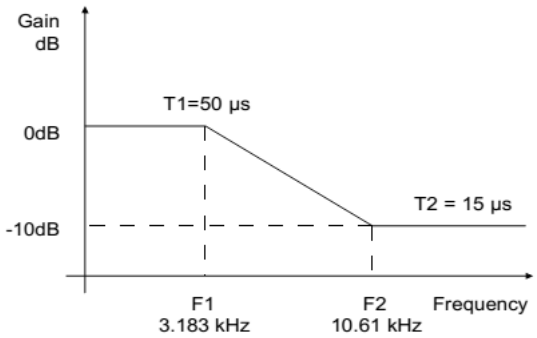


Figure 19. De-Emphasis Curve

8.2.4 Functional Mode (FM1:0) BITs 1-0

Default = 00
00 - Single-Speed Mode (30 to 50 kHz sample rates)
01 - Double-Speed Mode (50 to 100 kHz sample rates)
10 - Quad-Speed Mode (100 to 200 kHz sample rates)
11 - Direct Stream Digital Mode

Function:

Selects the required range of input sample rates or DSD Mode.

8.3 Volume Mixing and Inversion Control - Register 03h

7	6	5	4	3	2	1	0
VOLB=A	INVERT A	INVERT B	ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0
0	0	0	0	1	0	0	1

8.3.1 Channel B Volume = Channel A Volume (VOLB=A) Bit 7

Function:

When set to 0 (default), the AOUTA and AOUTB volume levels are independently controlled by the A and the B Channel Volume Control Bytes.

When set to 1, the volume on both AOUTA and AOUTB are determined by the A Channel Attenuation and Volume Control Bytes, and the B Channel Bytes are ignored.

8.3.2 Invert Signal Polarity (Invert_A) Bit 6

Function:

When set to 1, this bit inverts the signal polarity of channel A.

When set to 0 (default), this function is disabled.

8.3.3 Invert Signal Polarity (Invert_B) Bit 5

Function:

When set to 1, this bit inverts the signal polarity of channel B.

When set to 0 (default), this function is disabled.

8.3.4 ATAPI Channel Mixing and Muting (ATAPI4:0) Bits 4-0

Default = 01001 - AOUTA=aL, AOUTB=bR (Stereo)

Function:

The M9000 implements the channel-mixing functions of the ATAPI CD-ROM specification. Refer to Table and Figure 19 for additional information.

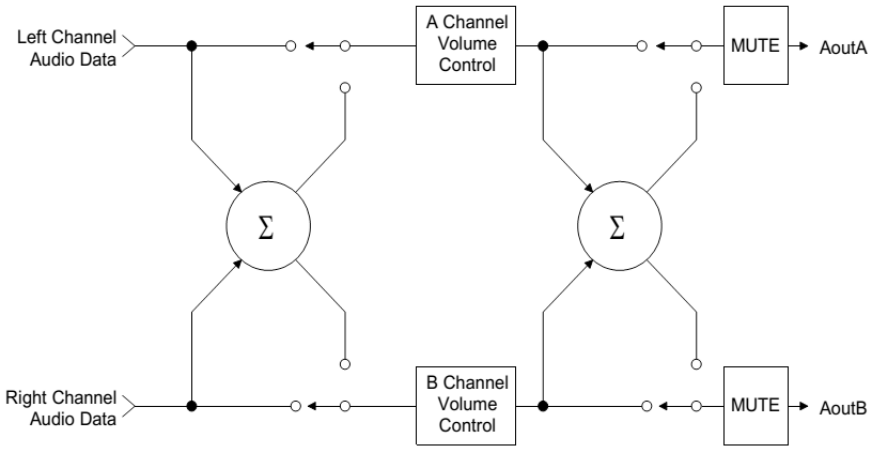


Figure 20. ATAPI Block Diagram

ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0	AOUTA	AOUTB
0	0	0	0	0	MUTE	MUTE
0	0	0	0	1	MUTE	bR
0	0	0	1	0	MUTE	bL
0	0	0	1	1	MUTE	b[(L+R)/2]
0	0	1	0	0	aR	MUTE
0	0	1	0	1	aR	bR
0	0	1	1	0	aR	bL
0	0	1	1	1	aR	b[(L+R)/2]
0	1	0	0	0	aL	MUTE
0	1	0	0	1	aL	bR
0	1	0	1	0	aL	bL
0	1	0	1	1	aL	b[(L+R)/2]
0	1	1	0	0	a[(L+R)/2]	MUTE
0	1	1	0	1	a[(L+R)/2]	bR
0	1	1	1	0	a[(L+R)/2]	bL
0	1	1	1	1	a[(L+R)/2]	b[(L+R)/2]
1	0	0	0	0	MUTE	MUTE
1	0	0	0	1	MUTE	bR
1	0	0	1	0	MUTE	bL
1	0	0	1	1	MUTE	b[(L+R)/2]
1	0	1	0	0	aR	MUTE
1	0	1	0	1	aR	bR
1	0	1	1	0	aR	bL
1	0	1	1	1	aR	[(aL+bR)/2]
1	1	0	0	0	aL	MUTE
1	1	0	0	1	aL	bR
1	1	0	1	0	aL	bL
1	1	0	1	1	aL	[(aL+bR)/2]
1	1	1	0	0	[(aL+bR)/2]	MUTE
1	1	1	0	1	[(aL+bR)/2]	bR
1	1	1	1	0	[(bL+aR)/2]	bL
1	1	1	1	1	[(aL+bR)/2]	[(aL+bR)/2]

8.4 Mute Control - Register 04h

7	6	5	4	3	2	1	0
PAMUTE	DAMUTE	MUTEC A=B	MUTE_A	MUTE_B	Reserved	MUTEP1	MUTEP0
1	1	0	0	0	0	0	0

8.4.1 PCM Auto-Mute (PAMUTE) Bit 7

Function:

When set to 1 (default), the Digital-to-Analog converter output will mute following the reception of 8192

consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained, and the Mute Control pin will go active during the mute period.

When set to 0, this function is disabled.

8.4.2 DSD Auto-Mute (DAMUTE) Bit 6

Function:

When set to 1 (default), the Digital-to-Analog converter output will mute following the reception of 256 repeated 8-bit DSD mute patterns (as defined in the SACD specification).

A single bit not fitting the repeated mute pattern (mentioned above) will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained, and the Mute Control pin will go active during the mute period.

When set to 0, this function is disabled.

8.4.3 AMUTEC = BMUTEC (MUTEC A=B) Bit 5

Function:

When set to 0 (default), the AMUTEC and BMUTEC pins operate independently.

When set to 1, the individual controls for AMUTEC and BMUTEC are internally connected through an AND gate prior to the output pins. Therefore, the external AMUTEC and BMUTEC pins will go active only when the requirements for both AMUTEC and BMUTEC are valid.

8.4.4 A Channel Mute (MUTE_A) Bit 4
B Channel Mute (MUTE_B) Bit 3

Function:

When set to 1, the Digital-to-Analog converter output will mute. The quiescent voltage on the output will be retained. The muting function is affected, similar to attenuation changes, by the Soft and Zero Cross bits in the Volume and Mixing Control register. The corresponding MUTEC pin will go active following any ramping due to the soft and zero cross function.

When set to 0 (default), this function is disabled.

8.4.5 MUTE Polarity and DETECT (MUTEP1:0) Bits 1-0

Default = 00
00 - Auto polarity detect, selected from AMUTEC pin
01 – Reserved
10 - Active low mute polarity
11 - Active high mute polarity

Function:

Auto mute polarity detect (00)

See section 6.3 on page "6.3 Format Selection" on page 25 for description.

Active low mute polarity (10)

When $\overline{RST}$ is low, the outputs are high-impedance and will need to be biased active. Once reset has been released and after this bit is set, the MUTEC output pins will be active low polarity.

Active high mute polarity (11)

At reset time, the outputs are high-impedance and will need to be biased active. Once reset has been released and after this bit is set, the MUTEC output pins will be active high polarity.

8.5 Channel A Volume Control - Register 05h

8.6 Channel B Volume Control - Register 06h

7	6	5	4	3	2	1	0
VOL7	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
0	0	0	0	0	0	0	0

8.6.1 Digital Volume Control (VOL7:0) Bits 7-0

Default = 00h (0 dB)

Function:

The Digital Volume Control registers allow independent control of the signal levels in 1/2 dB increments from 0 to -127.5 dB. Volume settings are decoded as shown in **Table 7**. The volume changes are implemented as dictated by the Soft and Zero Cross bits in the Power and Muting Control register. Note that the values in the volume setting column in Table 7 are approximate. The actual attenuation is determined by taking the decimal value of the volume register and multiplying by 6.02/12.

Binary Code	Decimal Value	Volume Setting
00000000	0	0 dB
00000001	1	-0.5 dB
00000110	6	-3.0 dB
11111111	255	-127.5 dB

Table 7. Example Digital Volume Settings

8.7 Ramp and Filter Control - Register 07h

7	6	5	4	3	2	1	0
SZC1	SZC0	RMP_UP	RMP_DN	Reserved	FILT_SEL	Reserved	DIR_DSD
1	0	1	1	0	0	0	0

8.7.1 Soft Ramp and Zero Cross Control (SZC1:0) Bits 7-6

Default = 10

SZC1	SZC0	PCM Description	DSD Description
0	0	Immediate Change	Immediate Change
0	1	Zero Cross	
1	0	Soft Ramp	Soft Ramp
1	1	Soft Ramp on Zero Crossings	

Function:

Immediate Change

When Immediate Change is selected, all level changes will take effect immediately in one step.

Zero Cross

Zero Cross Enable dictates that signal-level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level-change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp PCM

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 8 left/right clock periods.

Soft Ramp DSD

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1 dB per 512 DSD_SCLK periods (1024 periods if 128x DSD_SCLK is used).

Soft Ramp and Zero Cross

Soft Ramp and Zero Cross Enable dictate that signal-level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a time-out period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

8.7.2 Soft Volume Ramp-Up after Error (RMP_UP) Bit 5

Function:

An un-mute will be performed after executing an LRCK/MCLK ratio change or error, and after changing the Functional Mode.

When set to 1 (default), this un-mute is affected, similar to attenuation changes, by the Soft and Zero Cross bits in the Volume and Mixing Control register.

When set to 0, an immediate un-mute is performed in these instances.

Notes: For best results, it is recommended that this feature be used in conjunction with the RMP_DN bit.

8.7.3 Soft Ramp-Down before Filter Mode Change (RMP_DN) Bit 4

Function:

If either the FILT_SEL or DEM bits are changed the DAC will stop conversion for a period of time to change its filter values. This bit selects how the data is affected prior to and after the change of the filter values.

When set to 1 (default), a mute will be performed prior to executing a filter mode change and an un-mute will be performed after executing the filter mode change. This mute and un-mute are affected, similar to attenuation changes, by the Soft and Zero Cross bits in the Volume and Mixing Control register.

When set to 0, an immediate mute is performed prior to executing a filter mode change.

Notes: For best results, it is recommended that this feature be used in conjunction with the RMP_UP bit.

8.7.4 Interpolation Filter Select (FILT_SEL) Bit 2

Function:

When set to 0 (default), the Interpolation Filter has a fast roll off.

When set to 1, the Interpolation Filter has a slow roll off.

The specifications for each filter can be found in the Analog characteristics table, and response plots can be found in **Figure 23** to **Figure 46** in the “Appendix” on page "11. Appendix" on page 43.

8.7.5 Direct DSD Conversion (DIR_DSD) Bit 0

Function:

When set to 0 (default), DSD input data is sent to the DSD processor for filtering and volume control functions.

When set to 1, DSD input data is sent directly to the switched capacitor DACs for a pure DSD conversion. In this mode, the full-scale DSD and PCM levels will not be matched (see Section 3), the dynamic range performance may be reduced, the volume control is inactive, and the 50 kHz low pass filter is not available (see Section 3 for filter specifications).

8.8 Misc. Control - Register 08h

7	6	5	4	3	2	1	0
PDN	CPEN	FREEZE	MCLKDIV2	MCLKDIV3	Reserved	Reserved	Reserved
1	0	0	0	0	0	0	0

8.8.1 Power Down (PDN) Bit 7

Function:

When set to 1 (default), the entire device enters a low-power state, and the contents of the control registers is retained. The power-down bit defaults to '1' on power-up and must be disabled before normal operation in Control Port mode can occur. This bit is ignored if CPEN is not set.

8.8.2 Control Port Enable (CPEN) Bit 6

Function:

This bit is set to 0 by default, allowing the device to power-up in Stand-Alone Mode. Control Port Mode can be accessed by setting this bit to 1. This allows operation of the device to be controlled by the registers, and the pin definitions will conform to Control Port Mode.

8.8.3 Freeze Controls (Freeze) Bit 5

Function:

When set to 1, this function allows modifications to be made to the registers without the changes taking effect until FREEZE is set back to 0. To make multiple changes in the Control Port registers take effect simultaneously, enable the FREEZE bit, make all register changes, then disable the FREEZE bit. When set to 0 (default), register changes take effect immediately.

8.8.4 Master Clock Divide-by-2 ENABLE (MCLKDIV2) Bit 4

Function:

When set to 1, the MCLKDIV bit enables a circuit which divides the externally applied MCLK signal by 2 prior to all other internal circuitry.

When set to 0 (default), MCLK is unchanged.

8.8.5 Master Clock Divide-by-3 ENABLE (MCLKDIV3) Bit 3

Function:

When set to 1, the MCLKDIV bit enables a circuit that divides the externally applied MCLK signal by 3 prior to all other internal circuitry.

When set to 0 (default), MCLK is unchanged.

8.9 Misc. Control - Register 09h

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	STATIC_DSD	INVALID_DSD	DSD_PM_MODE	DSD_PM_EN
0	0	0	0	1	0	0	0

8.9.1 Static DSD Detect (Static_DSD) Bit 3

Function:

When set to 1 (default), the DSD processor checks for 28 consecutive zeroes or ones and, if detected, sends a mute signal to the DACs. The MUTEC pins will eventually go active according to the DAMUTE register.

When set to 0, this function is disabled

8.9.2 Invalid DSD Detect (Invalid_DSD) Bit 2

Function:

When set to 1, the DSD processor checks for greater than 24 out of 28 bits of the same value and, if detected, will attenuate the data sent to the DACs. The MUTEC pins go active according to the DAMUTE register.

When set to 0 (default), this function is disabled.

8.9.3 DSD Phase Modulation Mode Select (DSD_PM_mode) Bit 1

Function:

When set to 0 (default), the 128Fs (BCKA) clock should be input to DSD_SCLK for phase modulation mode. (See **Figure 15** on page 24)

When set to 1, the 64Fs (BCKD) clock should be input to DSD_SCLK for phase modulation mode.

8.9.4 DSD Phase Modulation Mode Enable (DSD_PM_EN) Bit 0

Function:

When set to 1, DSD phase modulation input mode is enabled and the DSD_PM_MODE bit should be set accordingly.

When set to 0 (default), this function is disabled (DSD normal mode).

9. Parameter Definitions

Total Harmonic Distortion + Noise (THD+N)

THD+N is the ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full-scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

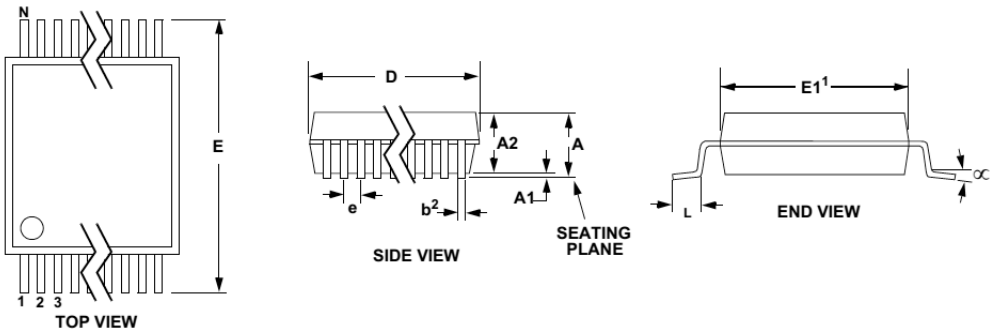
The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

10. Package Dimensions

10.1 28-TSSOP



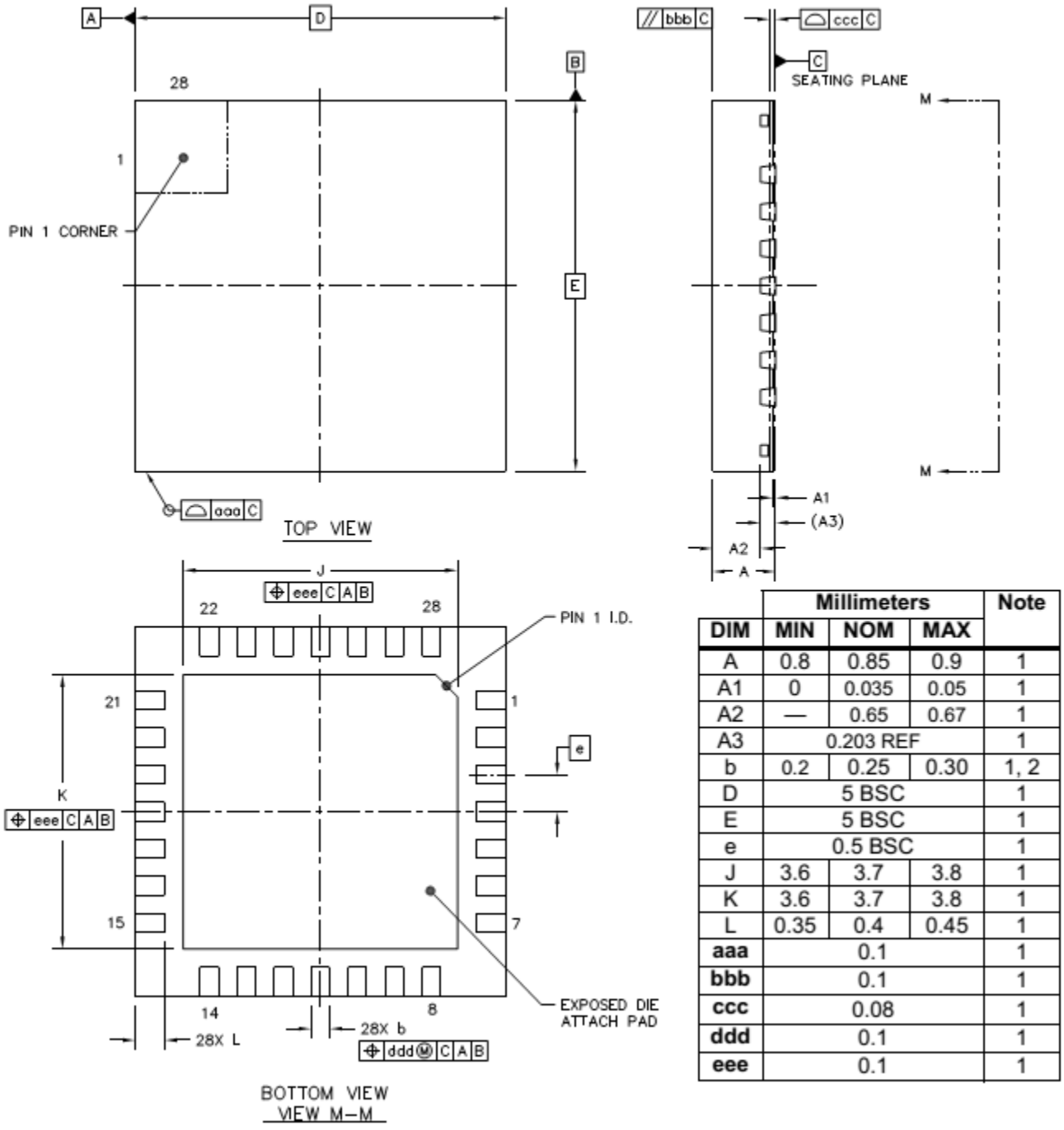
	Inches			Millimeters			Note
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**	
A	—	—	0.47	—	—	1.20	
A1	0.002	0.004	0.006	0.05	0.10	0.15	
A2	0.03150	0.035	0.04	0.80	0.90	1.00	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.378 BSC	0.382 BSC	0.386 BSC	9.60 BSC	9.70 BSC	9.80 BSC	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	—	0.026 BSC	—	—	0.65 BSC	—	
L	0.020	0.024	0.029	0.50	0.60	0.75	
µ	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153
Controlling Dimension is Millimeters.
Figure 21. 28L TSSOP (4.4 mm Body) Package Drawing

Notes:

1. "D" and "E1" are reference datums and do not include mold flash or protrusions, but do include mold mismatch and are measured at the parting line. Mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

10.2 28-QFN



DIM	Millimeters			Note
	MIN	NOM	MAX	
A	0.8	0.85	0.9	1
A1	0	0.035	0.05	1
A2	—	0.65	0.67	1
A3		0.203 REF		1
b	0.2	0.25	0.30	1, 2
D		5 BSC		1
E		5 BSC		1
e		0.5 BSC		1
J	3.6	3.7	3.8	1
K	3.6	3.7	3.8	1
L	0.35	0.4	0.45	1
aaa		0.1		1
bbb		0.1		1
ccc		0.08		1
ddd		0.1		1
eee		0.1		1

JEDEC #: MO-153
Controlling Dimension is Millimeters.
Figure 22. 28L QFN Package Drawing

Notes:

1. Dimensioning and tolerance per ASME Y 14.5M-1994.
2. Dimensioning lead width applies to the metalized terminal and is measured between 0.15 and 0.30 mm from the terminal tip.

Thermal Characteristics And Specifications

Parameters		Symbol	Min	Typ	Max	Units
Package Thermal Resistance (Note 3)	28-TSSOP	θ_{JA}	—	37	—	°C/Watt
		θ_{JC}	—	13	—	°C/Watt
	28-QFN	θ_{JA}	—	31	—	°C/Watt
		θ_{JC}	—	15	—	°C/Watt

3. θ_{JA} is specified according to JEDEC specifications for multi-layer PCBs.

11. Appendix

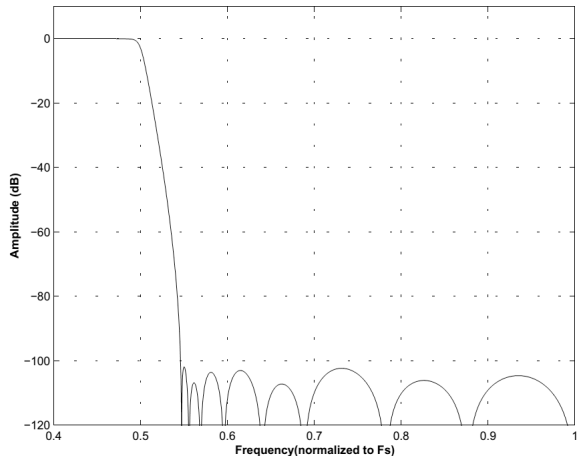


Figure 23. Single-Speed (fast) Stopband Rejection

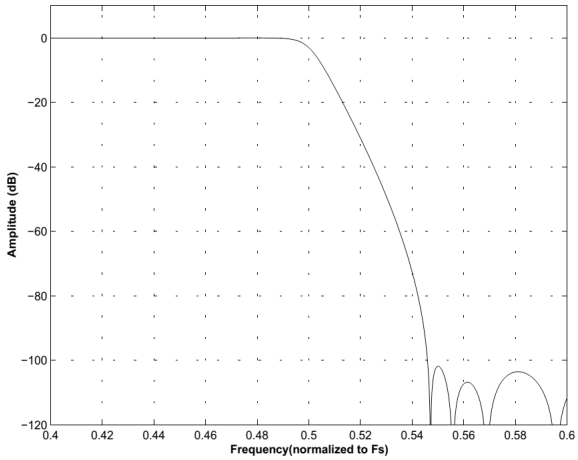


Figure 24. Single-Speed (fast) Transition Band

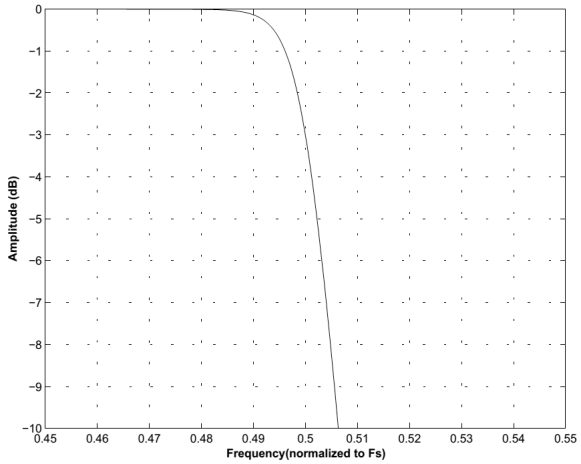


Figure 25. Single-Speed (fast) Transition Band (detail)

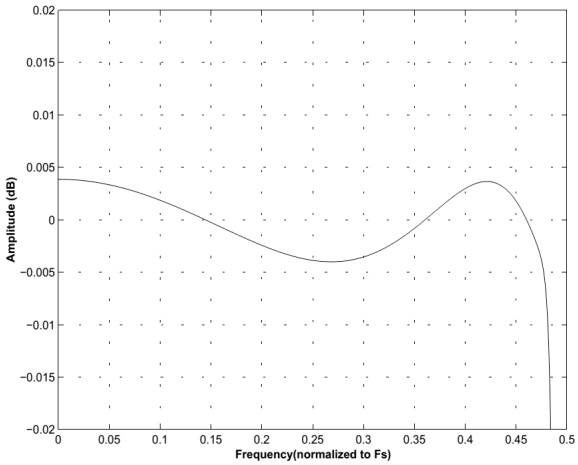


Figure 26. Single-Speed (fast) Passband Ripple

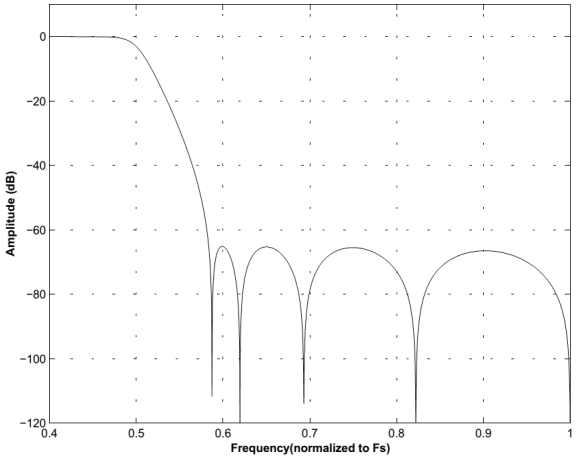


Figure 27. Single-Speed (slow) Stopband Rejection

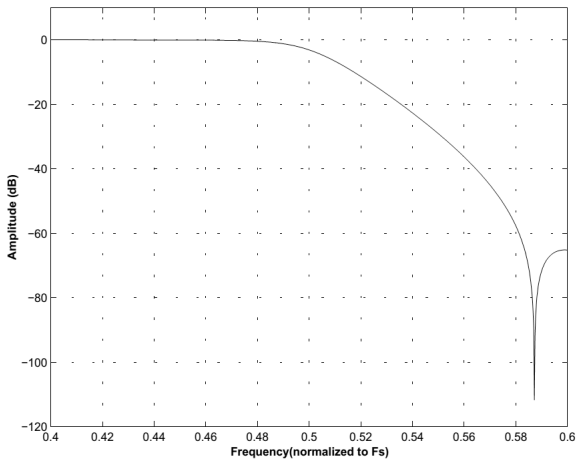


Figure 28. Single-Speed (slow) Transition Band

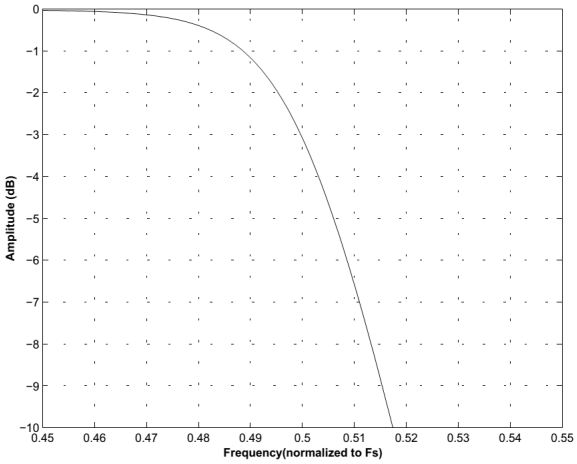


Figure 29. Single-Speed (slow) Transition Band (detail)

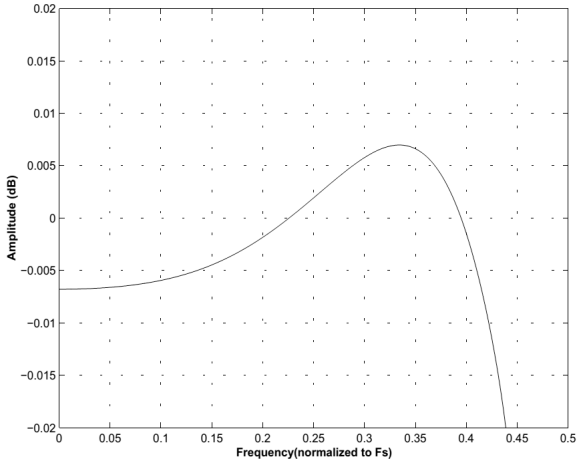


Figure 30. Single-Speed (slow) Passband Ripple

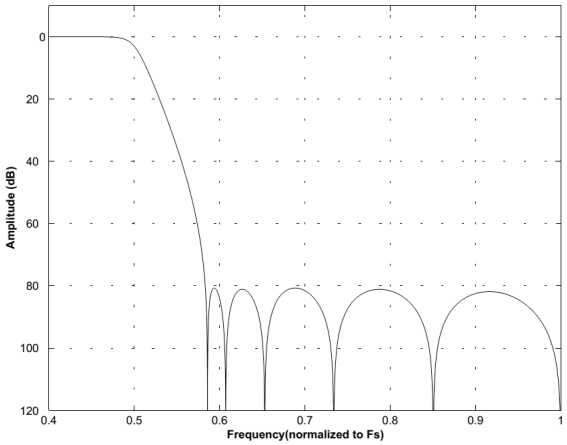


Figure 31. Double-Speed (fast) Stopband Rejection

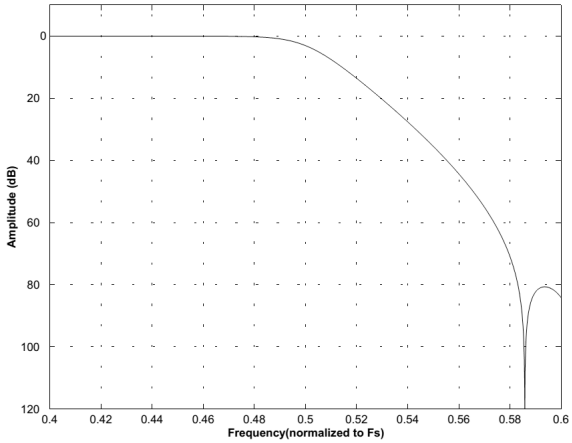


Figure 32. Double-Speed (fast) Transition Band

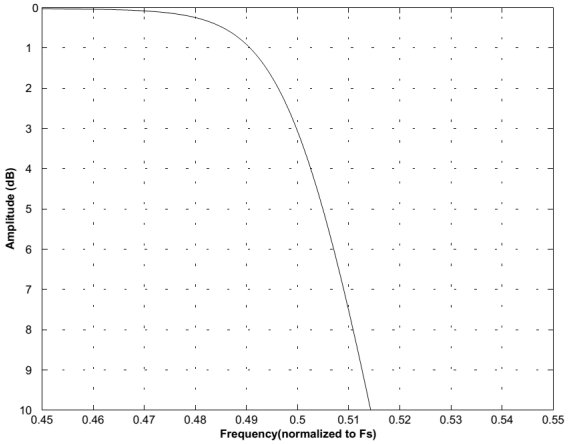


Figure 33. Double-Speed (fast) Transition Band (detail)

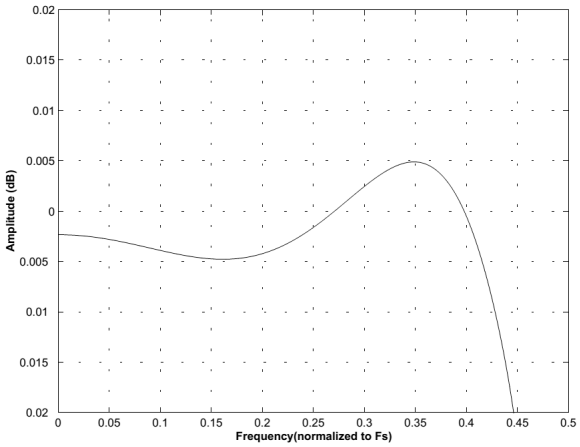


Figure 34. Double-Speed (fast) Passband Ripple

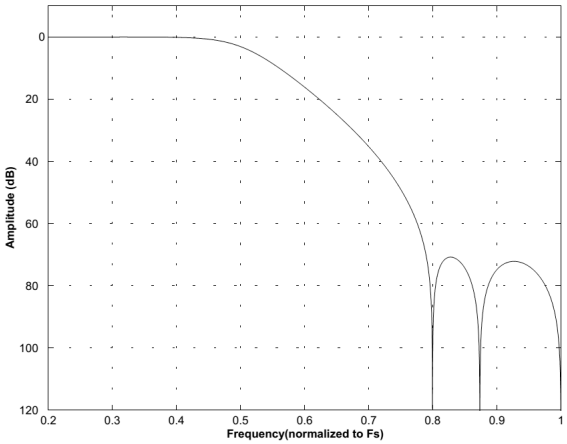


Figure 35. Double-Speed (slow) Stopband Rejection

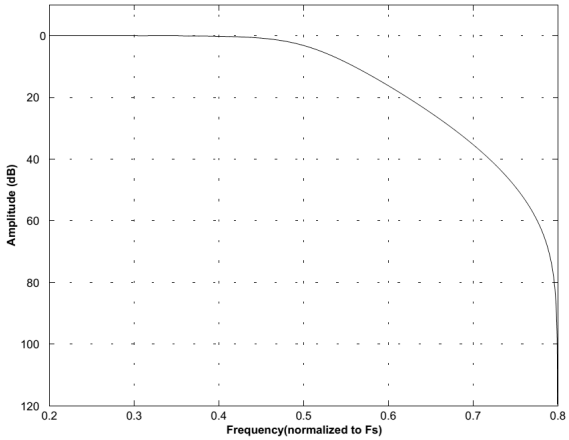


Figure 36. Double-Speed (slow) Transition Band

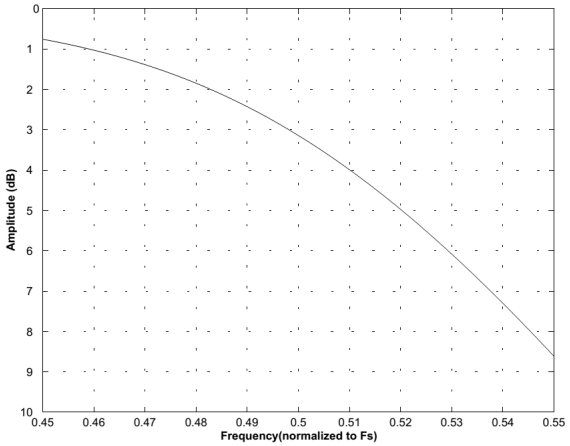


Figure 37. Double-Speed (slow) Transition Band (detail)

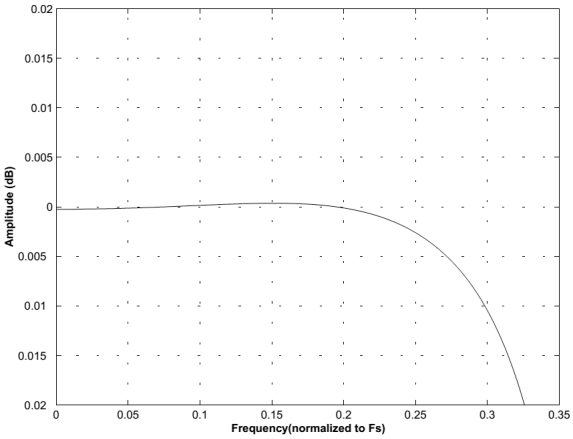


Figure 38. Double-Speed (slow) Passband Ripple

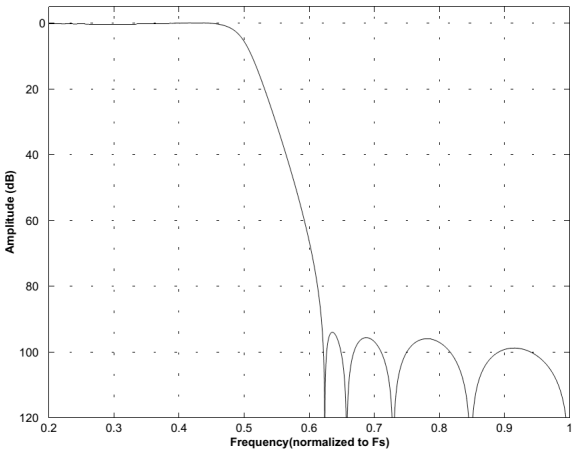


Figure 39. Quad-Speed (fast) Stopband Rejection

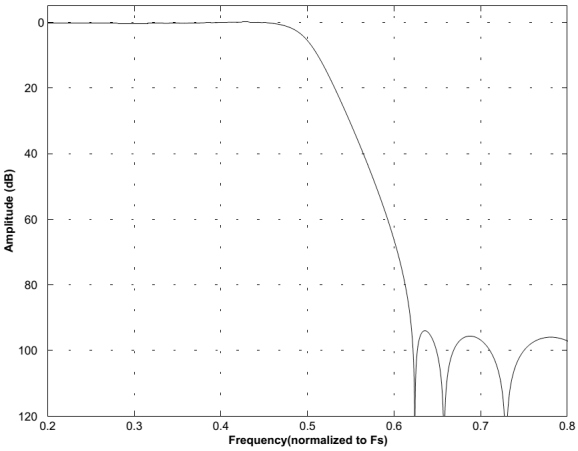


Figure 40. Quad-Speed (fast) Transition Band

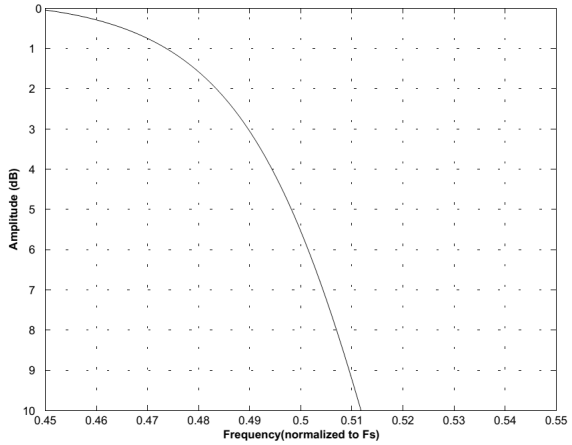


Figure 41. Quad-Speed (fast) Transition Band (detail)

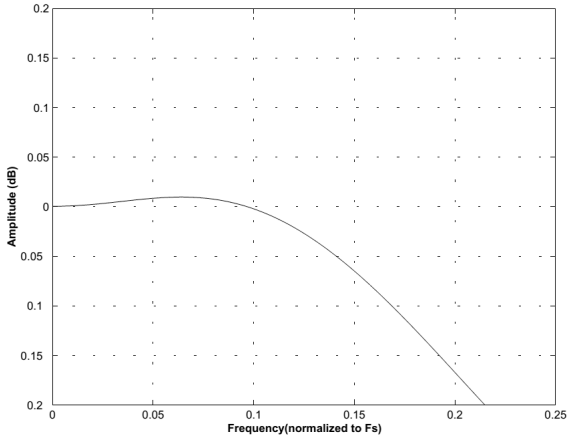


Figure 42. Quad-Speed (fast) Passband Ripple

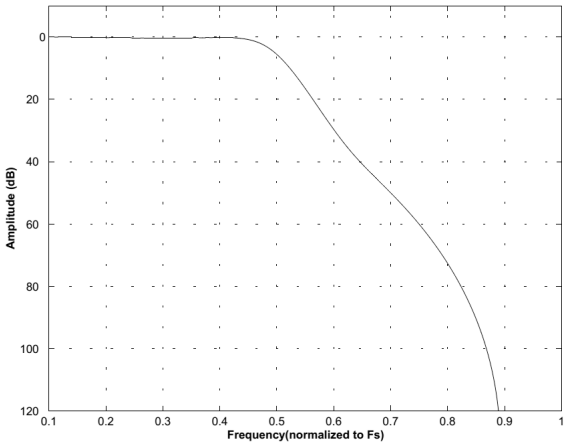


Figure 43. Quad-Speed (slow) Stopband Rejection

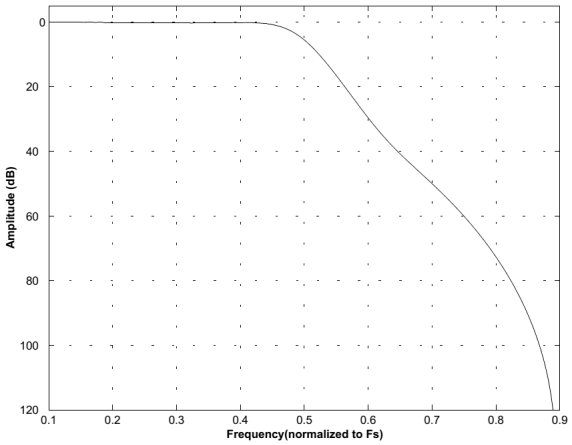


Figure 44. Quad-Speed (slow) Transition Band

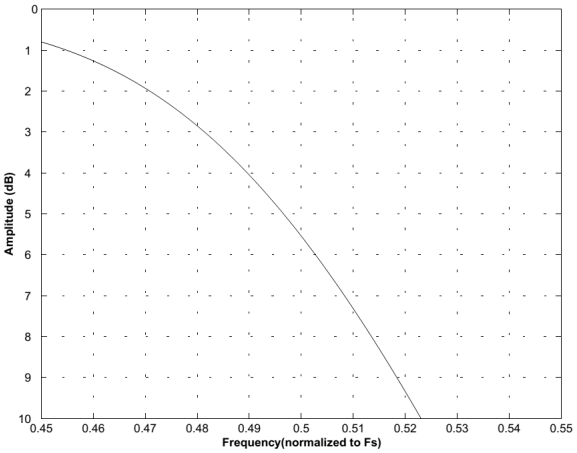


Figure 45. Quad-Speed (slow) Transition Band (detail)

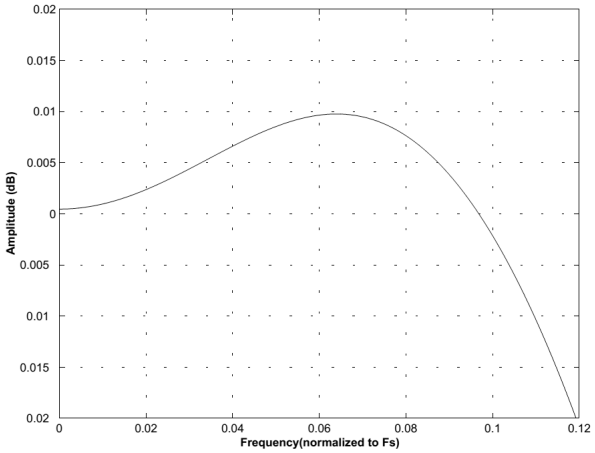


Figure 46. Quad-Speed (slow) Passband Ripple

12. Statements And Notes:

12.1 The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements					
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers
Lead frame	o	o	o	o	o	o
Plastic resin	o	o	o	o	o	o
Chip	o	o	o	o	o	o
The lead	o	o	o	o	o	o
Plastic sheet installed	o	o	o	o	o	o
explanation	o: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. x: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.					

12.2 Notion:

Recommended carefully reading this information before the use of this product;
The information in this document are subject to change without notice;
This information is using to the reference only, the company is not responsible for any loss;
The company is not responsible for the any infringement of the third party patents or other rights of the responsibility.