

# SSI2140

## FATKEYS™ VOLTAGE CONTROLLED MULTI-MODE FILTER

The SSI2140 is a new-generation voltage controlled filter that provides four highly-configurable variable transconductance cells for a wide variety of pole and mode combinations, and adds significant new features.

Based on an updated core by original SSM2040 designer Dave Rossum, the SSI2140 temperature compensates its transconductance cells for unprecedented stability. Temperature compensation is also optionally available for the exponential control.

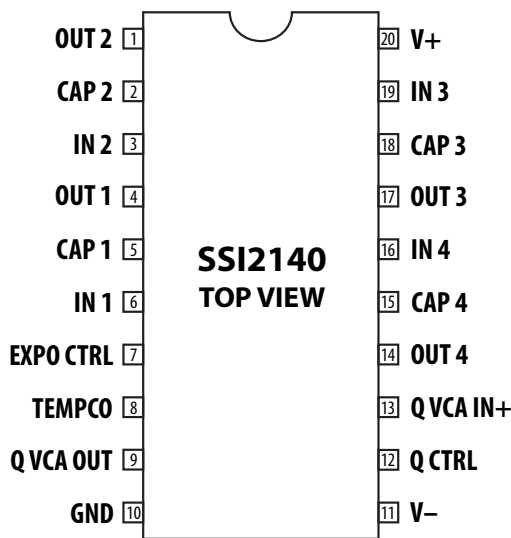
A temperature compensated VCA with linear control allows easy control of resonance and supports multiple Q compensation schemes, or otherwise can be used for traditional VCA/VCF roles.

Virtually any type of filter response from one to four poles can be achieved including low-pass, high-pass, band-pass, all-pass, notch, Sallen & Key, biquad, Cauer, state-variable, and others.

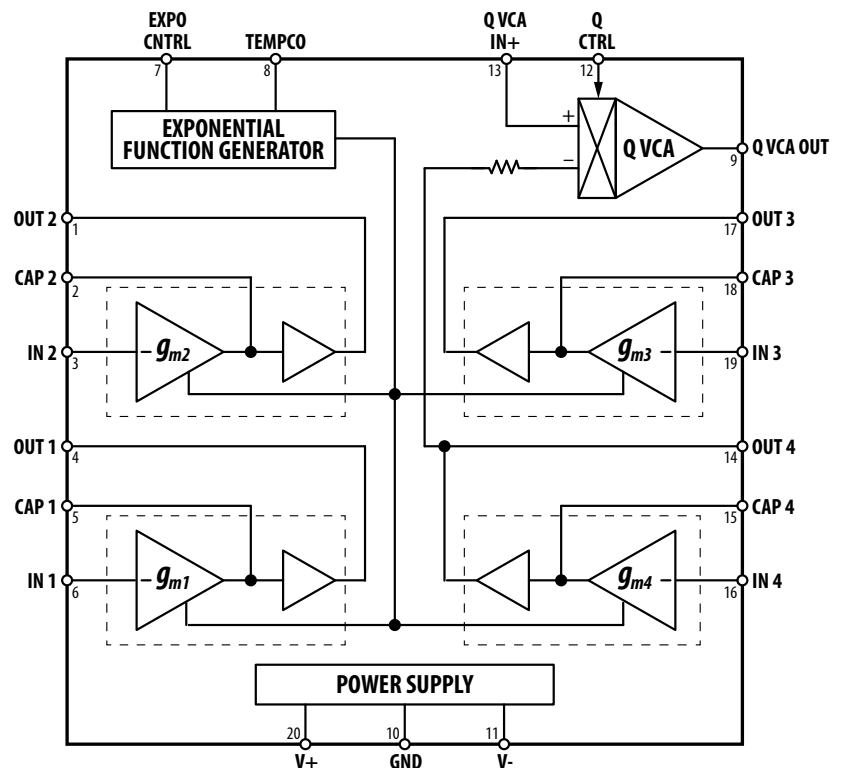
Most importantly, great care was taken to preserve the SSM2040's sonics including an input stage that can be overdriven for classic analog synthesizer character.

### FEATURES

- Highly Configurable Four-Section Filter
- Preserves SSM2040's Classic Filter Sound
- Exponential Frequency Control, with Optional Temperature Compensation
- On-Chip Resonance Circuit with Linear Control
- Optional Q Compensation
- ±4V to ±16V Operation
- Ultra-Compact 20-Lead SSOP Package



**PIN CONNECTIONS**  
20-LEAD SSOP



**FUNCTIONAL BLOCK**  
**DIAGRAM**

**SPECIFICATIONS** ( $V_S = \pm 12V$ ,  $f = 1kHz$ ,  $V_{IN} = V_{EXPO} = V_{QCTRL} = V_{QVIN+} = 0V$ ,  $T_A = 25^\circ C$ ; using Figure 1 and 3 circuits unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
Supply Voltage Range	$V_S$		$\pm 4$		$\pm 16$	V
Supply Current	$I_S$		$\pm 3.5$	$\pm 4.8$	$\pm 6.5$	mA
EXPO FUNCTION GENERATOR						
Frequency Control Sensitivity			-100	-18.4	+300	mV/oct
Frequency Control Input Range				90		mV
Frequency Control Input Bias Current						nA
Exponential Scale Factor Drift				+700		ppm/°C
Tempco Enabled				-3250		ppm/°C
Tempco Disabled						
Tempco Resistor Nominal Value			775	890	1000	$\Omega$
Tempco Resistor Temp. Coefficient				+3950		ppm/°C
TRANSCONDUCTANCE CELLS						
Transconductance	$G_M$	$V_{EXPO} = 0V$	160	215	270	$\mu S$
		$V_{EXPO} = -36mV$	700	850	1000	$\mu S$
Input Offset Voltage, Each Cell			0	0.65	2.0	mV
Change in Offset Voltage, Four Cells in Series		$\pm 5$ Octave Frequency Range		0.6		mV
Transconductance Temp. Coefficient				$\pm 200$		ppm/°C
Input Bias Current		$V_{EXPO} = 0V$		50		nA
Buffer Output Sink Current				1.6		mA
Buffer Output Source Current				10		mA
Equivalent Input Noise, Each Cell	$E_{IN}$	$V_{EXPO} = -90mV$ , 20Hz–20kHz		500		nV <sub>RMS</sub>
Passband Total Harmonic Distortion	THD	$V_{IN} = 1V_{P-P}$ , $V_{EXPO} = -90mV$		0.1		%
RESONANCE AND Q VCA						
Q Control Input Current Range	$I_Q$		0		500	$\mu A$
Q Control Current at Oscillation				222		$\mu A$
Q VCA Transconductance Coefficient	$K_{g_m}$		5.5	6.4	7.5	$\mu S/\mu A$
Q VCA Output Leakage				6.5		$\mu A$
Q VCA Input Bias Current		$V_{CTRL} = 222\mu A$		1.1	2.0	$\mu A$
Output Compliance			-0.3		$V_+ - 1.1$	V

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 18V$
Current into any Signal Pin	$\pm 5mA$
Max Voltage, any Pin (whichever is greater)	V- minus 0.3V V- plus 36V V+ plus 0.3V
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Operating Temperature Range	$-40^\circ C$ to $+85^\circ C$
Lead Temperature Range (Soldering, 10 sec)	$260^\circ C$

### ORDERING INFORMATION

Part Number	Package Type	Container
SSI2140SS-TU	20-Lead SSOP*, Tube Packing	76
SSI2140SS-RT	20-Lead SSOP*, Tape and Reel	4000

\*SSI Package ID "PSSL20"; mechanical drawing available at [www.sound-semiconductor.com](http://www.sound-semiconductor.com)

Features and specifications are subject to change without notice. While Sound Semiconductor strives to provide accurate and reliable information, no responsibility is assumed for use of its products, infringement of intellectual property, or other rights of third parties as a result of such use.

**PIN DESCRIPTIONS** (“x” refers to one of the four transconductance sections)

Pin(s)	Name	Description
1, 4, 14, 17	OUT x	Output of transconductance cell buffer amplifier. Limited to $\pm 1V$ swing, and can source 10mA and sink 1.6mA. 10k $\Omega$ or greater feedback and load resistors are recommended.
2, 5, 15, 18	CAP x	Integrating capacitor connected between CAP x and GND. To ensure stability, use values of 50pF or greater.
3, 6, 16, 19	IN x	Inverting input to variable transconductance amplifier. For optimum control rejection, the recommended input network is a 10k $\Omega$ input resistor with a 200 $\Omega$ attenuating resistor to GND.
7	EXPO CTRL	Control voltage that sets gain of the four transconductance amplifiers. The control response is exponential, with typical sensitivity of -18mV/octave.
8	TEMPCO	Internal 950 $\Omega$ (typical) temperature compensating resistor. If unused, leave disconnected.
9	Q VCA OUT	Output of the Q VCA.
10	GND	Connect to analog signal ground with short, low inductance trace.
11	V-	Negative supply. Recommend 100nF local decoupling capacitor placed as close to package as possible with a low inductance trace to ground.
12	Q CTRL	Controls gain of the Q VCA.
13	VCA IN+	Non-inverting input of the Q VCA. The inverting input is internally connected to OUT 4.
20	V+	Positive supply. Recommend 100nF local decoupling capacitor placed as close to package as possible with a low inductance trace to ground.

**USING THE SSI2140**

The SSI2140 contains four exponentially controlled transconductance (“ $g_m$ ”) cells with ultra-low bias current buffers. These cells and their associated buffers have been updated by the original designer to recreate audio characteristics of the acclaimed SSM2040 Voltage Controlled Filter, but include a few specific improvements:

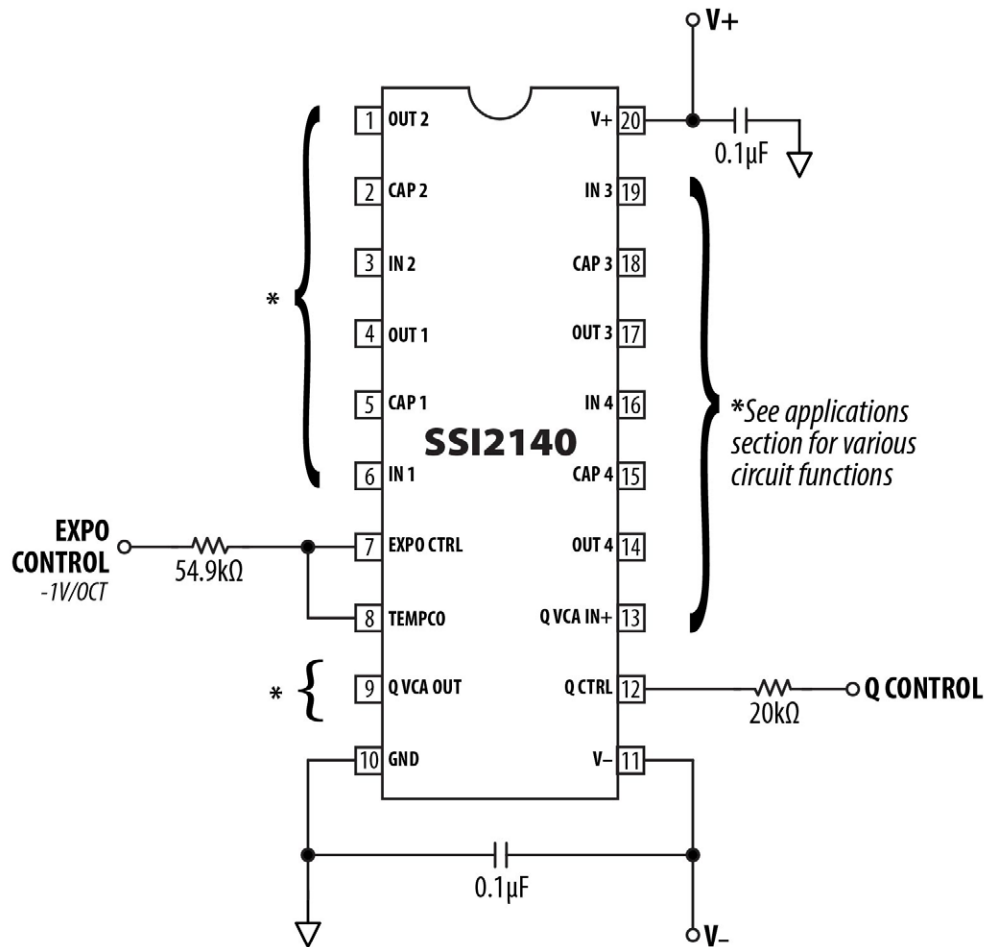
- The buffer bias current has been decreased by an order of magnitude, providing improved frequency control voltage rejection.
- Transistor geometries have been optimized for superior noise performance.
- The control circuitry has been temperature compensated to minimize the change of each cell’s  $g_m$  with die temperature variations.
- The transconductance at  $V_{EXPO} = 0V$  for the SSI2140 may vary slightly from the SSM2040. The SSM2040 was specified at typically 200 $\mu S$ , with a production variation range of 3:1. The SSI2140 has a nominal value of 190 $\mu S$ .

The SSI2140’s transconductance cells and the exponential generator can be considered otherwise identical to the SSM2040. The SSI2140 also contains additional circuitry not found in the SSM2040:

- A on-chip “tempco” resistor with a typical value of 950 $\Omega$  and a temperature coefficient of +3300ppm/ $^{\circ}C$ . This resistor, functionally similar to the TelLabs Q81, can optionally be used to temperature compensate the  $q/kT$  factor of the exponential generator.
- An on-chip temperature compensated VCA designed for use in controlling the resonance (“Q”) of a four pole low-pass filter configuration. The VCA’s connections have been designed to allow multiple options for “Q compensation” which counteracts the effect increased Q has on the filter’s DC gain. If the QVCA isn’t used for Q compensation it can be applied as a general-purpose VCA, for example as a high-pass filter.

**Typical Application Circuit**

Due to the SSI2140’s wide range of function, Figure 1 shows only those connections common to virtually all applications. Later sections describe various filter configurations and design ideas for the Q VCA.



**Figure 1: Common Connections for SSI2140**  
(Expo temperature compensation shown; see Figure 2 for uncompensated connection)

**Power Supplies**

The SSI2140 is normally powered from bipolar supplies ranging from  $\pm 4V$  to  $\pm 16V$ . For single-supply operation please refer to a later section. Supplies should be locally bypassed with 100nF ceramic capacitors placed close to the supply pins and short traces to ground. It is also recommended to provide larger bulk decoupling caps on each board, typically 47µF to 100µF per rail.

**Signal Inputs**

The four transconductance cells have a very limited input range – beyond 40mV peak-to-peak ( $\pm 20mV$ ) the input stage starts to distort. The recommended input scheme is a 10kΩ resistor from the signal source to the input pin, and a 200Ω resistor to ground. This reduces the signal down to the tens of millivolts that the input can handle, and sets the recommended peak input signal to  $2V_{P-P}$ .

Higher input levels overdrive the input stage, resulting in a distortion that many will find desirable. See [xxx] for further discussion.

**Signal Outputs**

The outputs of the transconductance cells are capable of driving 1V into a 5kΩ load. This is sufficient to drive the recommended 10kΩ feedback resistor and a 10kΩ input resistor to the next stage.

The Q VCA output is a current. If fed back to one of the transconductance cells, a direct connection can be made. For voltage output, a current-to-voltage converter op-amp is recommended as shown in the output gain compensated configuration in Figure 14.

**Exponential Frequency Control**

The frequency control pin has a typical sensitivity of -18mV per octave. It is recommended to use a series resistor together with a 1kΩ shunt resistor to attenuate external frequency control voltage down to this level. For example, for 1V per octave sensitivity use a 54.9kΩ series resistor and either an external 1kΩ shunt resistor or the internal tempco resistor. See Figure 2.

### Filter Capacitor Selection

For optimum audio performance use capacitors with low leakage and distortion. Ceramic COG/NPO, polystyrene, some polyester and polycarbonate types are recommended. The recommended value is 1nF. Smaller values will raise the cut off frequency and larger values will lower it; for example, 470pF capacitors will approximately double the cut off frequency, while 2.2nF will halve it.

The smallest recommended value is 50pF, and care must be taken with parasitic capacitance and leakage. Larger capacitance values are also possible, but cost may become prohibitive.

### Using the On-Chip Tempco Resistor

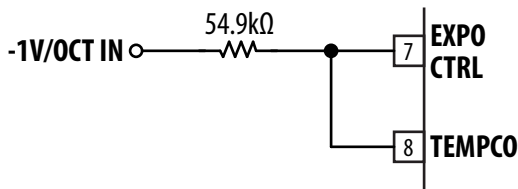
Pin 8 (TEMPCO) of the SSI2140 connects to an on-chip resistor whose other terminal is internally wired to ground. This resistor has a typical value of 900Ω and temperature coefficient of 3300ppm/°C.

Using this as a resistive attenuator will temperature compensate the SSI2140 exponential generator's inherent gain factor of q/kT by multiplying the input voltage by a factor proportional to the die temperature T in degrees Kelvin. The value of the input series resistor for a 1V/octave response is 54.9kΩ as shown in Figure 1.

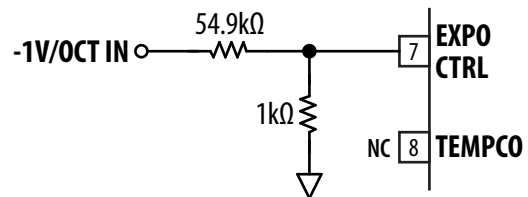
To take advantage of temperature compensation, simply tie pins 7 and 8 together. If the TEMPCO resistor is not used, pin 8 should be left open and a 1kΩ resistor added between pin 7 and ground to correctly scale the control voltage range. See Figure 2.

Note this resistor, being an on-chip implementation, has certain characteristics that differ from discrete resistors:

- It has a wide tolerance, typically ±25%. An appropriate 1V/octave trim range must be implemented.
- It is slightly non-linear, resulting in a modest deviation from the accuracy achievable by the internal exponential generator alone. Specifically, lower input voltages corresponding to higher cutoff and resonant frequencies will lower the resistor value causing the pitch to be slightly flatter than expected. This effect should be less than a semitone.
- The voltage across the resistor (at pin 8) should not exceed +300mV, as this will forward bias the resistor with respect to its surrounding well and the resistor may draw excessive current. There is no need for such a voltage at this pin under normal application.



2a: With On-Chip Temperature Compensation



2b: On-Chip Temperature Compensation Disabled

**Figure 2: TEMPCO Pin Connections**

### Resonance (Q) Control

The SSI2140 contains an internal current controlled amplifier that is temperature compensated for  $g_m$ . An external resistor turns this into a voltage controlled amplifier allowing easy scaling of control voltage range to Q control range. While this VCA has been designed and configured to control resonance of the filter in a four-pole low-pass configuration, its general purpose nature allows the creative designer great flexibility for other uses.

The Q VCA has a non-inverting low-level voltage input connected to pin 13 (Q VCA IN+) and a symmetric inverting input connected internally to the output of transconductance cell 4 by a 16:1 resistive divider. If the Q VCA is not used, Q VCA IN+ and Q VCA Out pins should be grounded and the Q CNTL pin 12 left open.

The Q CNTL pin is a ground-referenced current input. For simple CV control a single resistor is needed; with the recommended value of 20kΩ a control voltage of 4.4V results in oscillation when used to control filter Q, and 0V equals zero resonance.

The transconductance of the VCA is typically 30μS/μA. For oscillation in a four-pole configuration, where each stage contributes 3dB attenuation, the loop gain should be 12dB. The filter's loop gain is given by the following expression:

$$G_{Loop} = \frac{G_{VCAInput} K_{G_m} I_Q R_Q}{G_{FilterInput}}$$

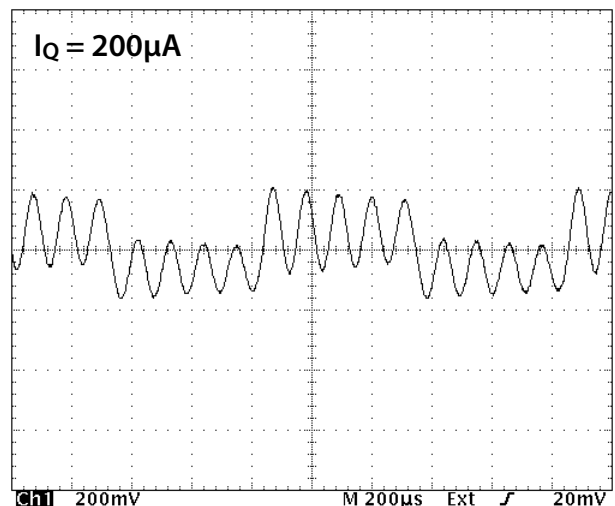
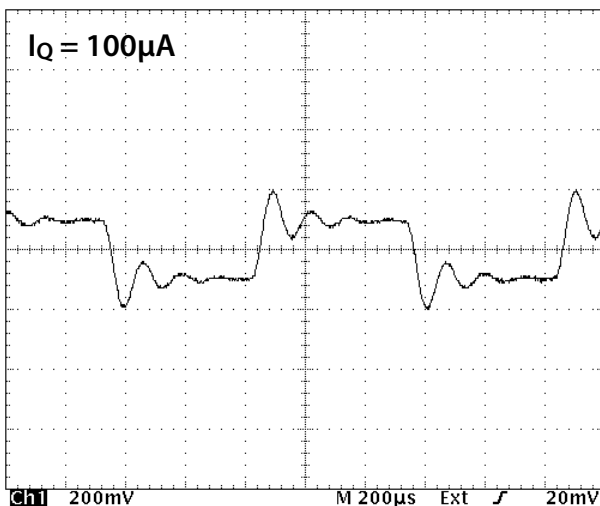
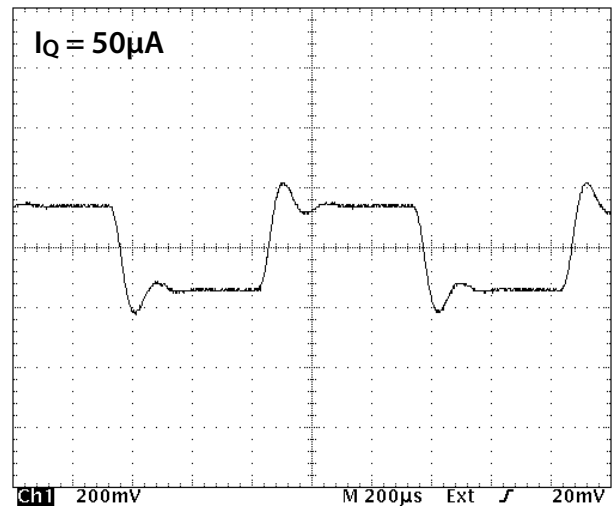
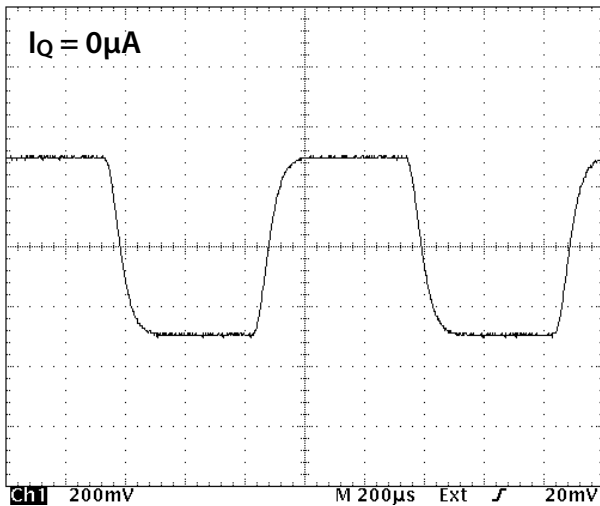
where  $G_{Loop}$  is the loop gain,  $G_{FilterInput}$  is the gain of the resistive divider network at the filter input,  $G_{VCAInput}$  is the gain of the resistive divider network at the VCA input,  $K_{gm}$  is the  $g_m$  constant of the VCA,  $I_Q$  is the VCA control current, and  $R_Q$  is the resistor on the output of the VCA (typically 200 Ohms). Re-arranging for  $I_Q$  we get the following expression:

$$I_Q = \frac{G_{Loop} G_{FilterInput}}{G_{VCAInput} K_{G_m} R_Q}$$

For oscillation the loop gain needs to be 12dB ( $\times 3.981$ ). The SSI2140 Q VCA has a 16:1 input attenuator. For the typical low-pass filter shown in Figure 3 the filter input attenuator is a 10k:200 resistor network, and  $R_Q$  is also the lower 200Ω resistor. Putting these figures into the above equation produces a VCA control current requirement of 221μA:

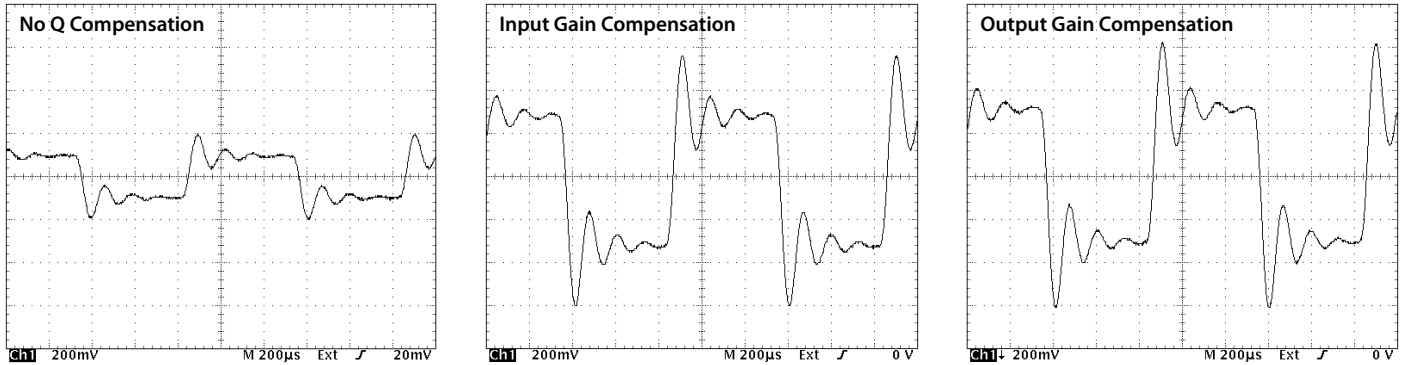
$$I_Q = \frac{3.981 \times \frac{200}{10k + 200}}{\frac{1k}{16k + 1k} \times 30 \times 200} = 221 \mu A$$

The plots below show a 1kHz 600mV<sub>p-p</sub> square wave input signal applied to the typical application circuit against different Q control currents. Two points to note are that the overall amplitude drops as resonance increases, and when  $I_Q$  is 200μA the filter is very close to resonance.



### Q Compensation

The arrangement of the Q control circuit determines the type and degree of Q Compensation. Various configurations are described further in "Filter Design Notes." Plotted below are low-pass filter outputs for the two Q compensation schemes from a 1kHz square wave input and  $I_Q = 100\mu A$ . The no-compensation plot for the same  $I_Q$  is shown for comparison.



### TYPICAL APPLICATION: FOUR-POLE LOW-PASS FILTER

A typical application of the SSI2140 is shown in Figure 3. The input signal is fed via a 10kΩ resistor into the summing node. The reduced voltage across the 200Ω resistor is fed into the first transconductance cell's input pin. The voltage is then converted to a current according to the transconductance of the cell. Current accumulates on the 1000pF capacitor, producing a voltage which is buffered and provided at the output pin.

To construct a low-pass filter, a proportion of the output signal is fed back to the input. As the buffer is inverting, the output is of the opposite polarity to the input, and eventually the loop around the transconductance cell will stabilize according to the DC component of the input signal. This is the classic low-pass filter operation.

The output of the first stage is then fed into the next stage in exactly the same way, and so on for the remaining stages. The final output of the filter is taken from the output of the fourth transconductance buffer.

A proportion of the final output signal is also fed back to the input through the Q VCA. When the Q VCA is off, no signal is fed back to the input. As the Q VCA control voltage increases, an increasing amount of output signal is fed back to the input. At the cut off frequency the phase shift through each transconductance cell is 45 degrees, culminating in a total phase shift of 180 degrees. The output of the fourth stage then feeds into the inverting input of the Q VCA, giving a further 180 degrees phase shift. All together the 360 degrees phase shift enhances the output signal level at the cutoff frequency, giving rise to the classic peaking of the filter output.

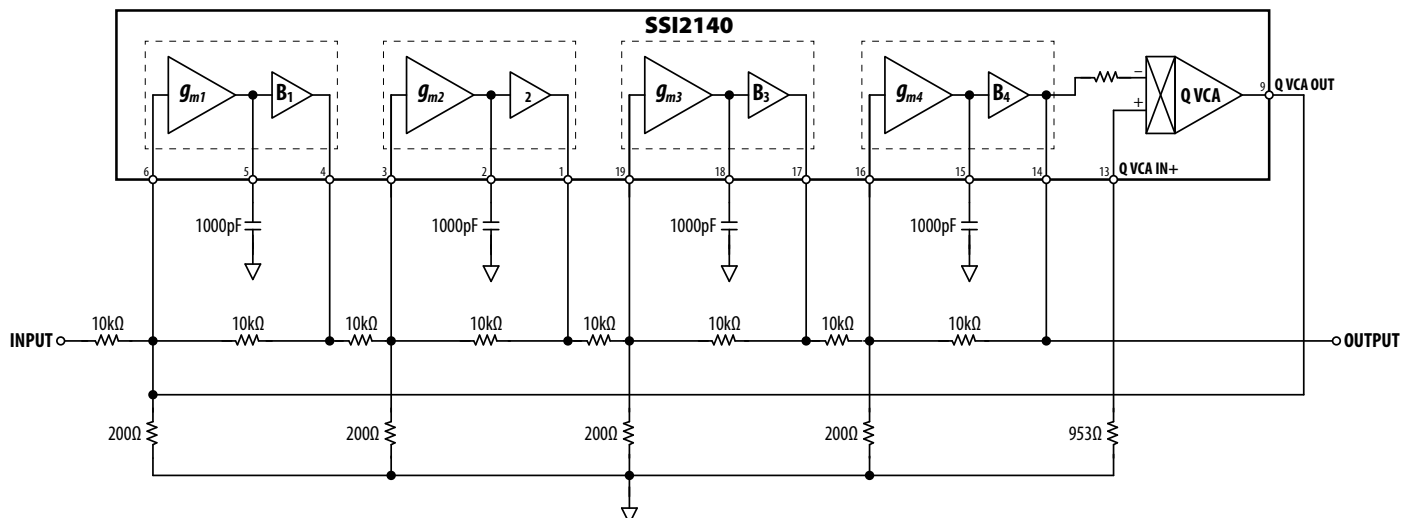


Figure 3: Four-Pole Low-Pass Filter with No Q Compensation



As the gain of the Q VCA is increased further the amount of feedback becomes sufficient to sustain oscillation of the filter. If amplitude control is implemented then it is possible to construct a low distortion sine wave oscillator whose frequency is controlled by the cutoff control. In this way it is possible to add an additional oscillator – albeit sine wave only – to a music synthesizer.

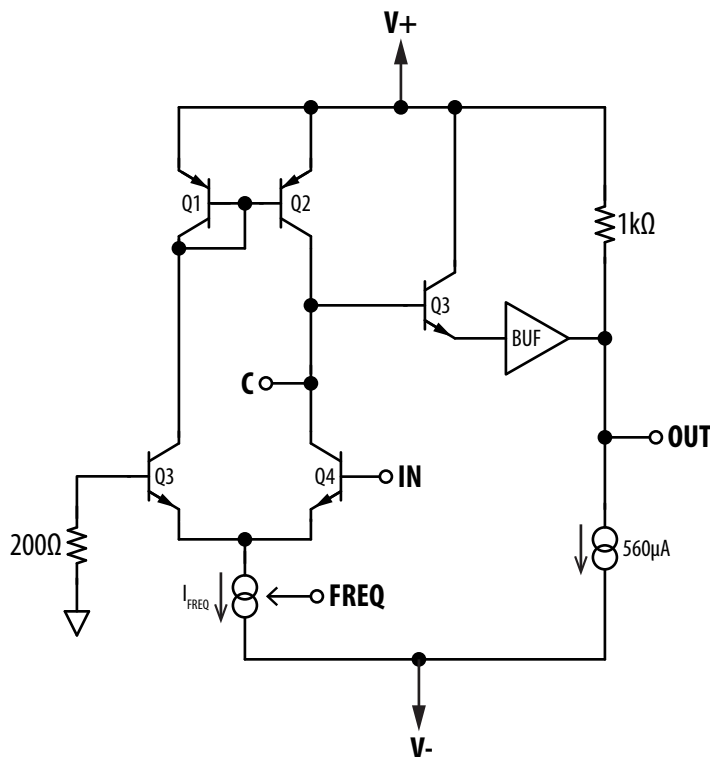
The configuration shown in Figure 3 is the simplest, and provides no Q compensation. As in the classic electronic music four-pole lowpass filter, the passband (DC) gain decreases with increasing Q proportional with the gain of the Q VCA. Near oscillation, the passband is attenuated by 12dB – an effect traditional synthesizer enthusiasts are accustomed to. Others prefer to avoid the passband attenuation effect, which is easily solved by the SSI2140's QVCA as demonstrated on Page 7 and described in detail later.

**PRINCIPLES OF OPERATION**

The SSI2140 comprises four variable transconductance cells sharing a common control port, plus a temperature compensated current controlled variable gain amplifier.

**Transconductance Amplifier**

A simplified schematic of the transconductance cells is shown in Figure 4. Each cell comprises a variable transconductance amplifier followed by a high input-resistance buffer.



**Figure 4: SSI2140 Simplified Circuit – Transconductance Cell and Buffer**

Transistors Q1 and Q2 are a current mirror and provide an active load for the differential pair Q3 and Q4. The input to the transconductance amplifier is the voltage applied to the base of Q4. The base of Q3 is tied to ground through a 200Ω resistor.

When the input is 0V, both transistor bases are at the same potential so the same current flows through both Q3 and Q4. The total current, set by current source  $I_{FREQ}$  (controlled by the EXPO CTRL pin), is shared equally between Q3 and Q4. As  $I_{FREQ}/2$  flows into the collector of Q3, by mirror action an equal but opposite current flows out of the collector of Q2. This current exactly balances the current flowing into Q4's collector, and so there is no current flowing into or out of the C terminal. Assuming a capacitor is connected to this terminal, the voltage across the capacitor does not change.

A small positive voltage applied to the base of Q4 causes it to pass more current according to Q4's transconductance. Because  $I_{FREQ}$  is held constant this results in less current flowing into Q3's collector. Action of the Q1/Q2 current mirror also reduces the current flowing out of Q2's collector. An imbalance causes a current to flow into the C pin, resulting in the voltage across the external capacitor falling at a constant rate, the slope of which is determined by the value of the capacitor and the magnitude of the current flowing out of the capacitor according to:



$$V_c = \frac{1}{C} \int i_c dt$$

where  $i_c$  is the output current of the transconductance cell,  $C$  is the value of the capacitor, and  $V_c$  is the voltage developed across the capacitor that is then buffered and provided at the output pin. For small negative voltages a similar operation occurs but in the opposite direction.

The ratio between the input voltage and output current (" $g_m$ ") is set by  $I_{FREQ}$ , which is controlled by a voltage on the EXPO CTRL pin. In a filter circuit this results in the cutoff frequency of each transconductance cell being adjustable over a wide range.

For best control feedthrough rejection the impedances seen by the bases of Q3 and Q4 must be the same. The base of Q3 is internally connected to GND through a 200Ω resistor, so the designer should aim to present a similar impedance to the base of Q4. The recommended circuit, with a 200Ω resistor to GND, satisfies this requirement; the effect of the 10kΩ input resistors is minimal.

### Output Buffer

The voltage at the C pin is sensed by emitter follower Q5, before driving the buffer circuit BUF (the circuit inside the buffer is not shown). The output of BUF looks like a 1kΩ resistor to  $V+$  and a 560μA current sink to  $V-$ . This results in an asymmetric output drive: the output can source up to 11.4mA (when  $V+ = +12V$ ) but only sink up to 560μA.

Because the input signal is connected to the inverting input of the transconductance amplifier, and the output buffer is non-inverting, each transconductance cell inverts the input signal. This is important for pole mixing applications where the output is some weighted sum of the individual outputs.

### Current Controlled Amplifier

The variable Q control is performed by a current-controlled amplifier shown in Figure 5.

The behavior of the current controlled amplifier is similar to the transconductance cells. Transistors Q1 and Q2 form a current mirror active load for differential transistor pair Q3 and Q4. The gain of the amplifier is set by the emitter currents which are set by the temperature-compensated current source. This current source is controlled by the externally-applied control current flowing into the ground-referenced Q CTRL pin.

The Q VCA has two inputs. The non-inverting input, at the base of Q3, is connected to the Q VCA IN+ pin. The inverting input, at the base of Q4, is internally connected through a 16kΩ/1kΩ resistive divider, to the output of the fourth transconductance cell. Again, for minimal control feedthrough the impedances seen by both inputs should be the same.

The output current is taken from the junction between the collectors of Q2 and Q4. For correct operation this pin must be kept at ground, either with an external op-amp configured to generate a virtual ground or, if not required, it can be directly connected to ground.

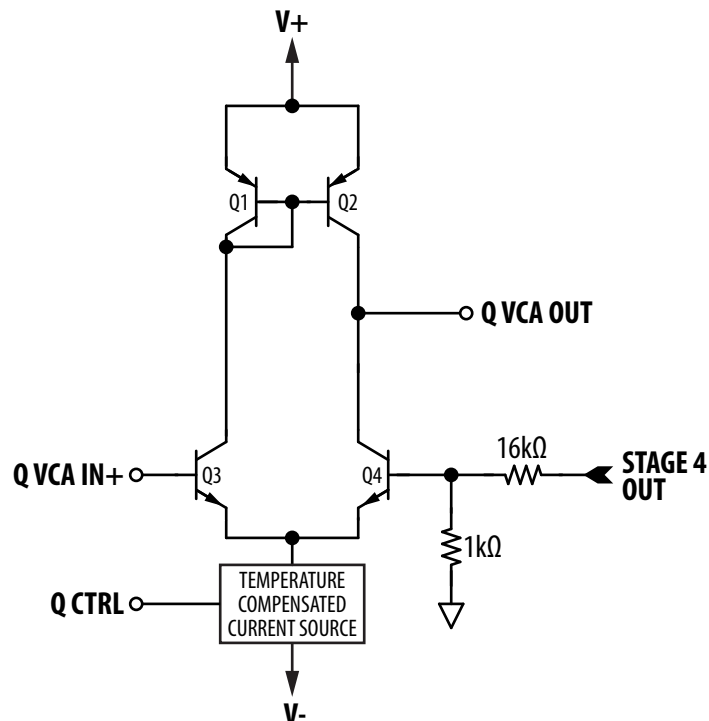


Figure 5: SSI2140 Simplified Circuit – Q VCA

### Temperature Compensation

All semiconductor devices are sensitive to temperature. The SSI2140 includes three temperature compensation schemes. Firstly, the QVCA automatically compensates for changes in the temperature of the IC, requiring no external connections. Secondly, the SSI2140 automatically compensates for the temperature variation of the transconductances of the four filter cells. Thirdly, an internal temperature-sensing element can be used to temperature-compensate the EXPO CTRL pin.

The compensation of the EXPO CTRL pin is provided by an internal 900Ω temperature-sensing resistor brought out to a pin adjacent to the EXPO CTRL pin and, together with a series resistor (54.9kΩ for 1V/oct), provides comprehensive temperature compensation. Its resistance at 25°C is typically 900Ω. However when the SSI2140 is powered the part dissipates around 120mW, heating up the silicon by about 20°C above ambient temperature. This increases the value of this resistor to about 1kΩ during normal operation, and which tracks the ambient temperature.

Temperature compensation of the EXPO CTRL pin is less useful in microprocessor-controlled polyphonic synthesizers, which may prefer to run regular tuning cycles to track temperature and keep all voices in tune together.

## APPLICATION INFORMATION

### FILTER DESIGN NOTES

Frequency control of all four SSI2140 transconductance cells is governed by the voltage at EXPO CTRL, which is described by:

$$G = 190\mu S \times 2^{\frac{-V_{EXPO}}{0.018}}$$

Filter Type	Gain (A)	F <sub>c</sub>	Q	Transfer Function
Low-Pass - Real Pole	$\frac{-R2}{R1}$	$\frac{200G}{2\pi R2C}$	$\frac{1}{2}$	$\frac{-A}{(S+1)}$
High-Pass - Real Pole	1	$\frac{200G}{2\pi RC}$	$\frac{1}{2}$	$\frac{S}{(S+1)}$
All-Pass	1	$\frac{200G}{2\pi RC}$	$\frac{1}{2}$	$\frac{S-1}{(S+1)}$
Sallen & Key Low-Pass	$\frac{R2}{R1}$	$\frac{200G}{2\pi R2C}$	$\frac{R3}{2R4}$	$\frac{A}{(S^2 + \frac{1}{Q}S + 1)}$
Sallen & Key High-Pass	1	$\frac{200G}{2\pi R1C}$	$\frac{R2}{2R3}$	$\frac{S^2}{(S^2 + \frac{1}{Q}S + 1)}$
Sallen & Key Band-Pass	$\frac{-R2}{R1}$	$\frac{200G}{2\pi R2C}$	$\frac{R3}{2R2}$	$\frac{-AS}{(S^2 + \frac{1}{Q}S + 1)}$
State Variable Low-Pass	$\frac{-R2}{R1}$	$\frac{200G}{2\pi R3C}$	$\frac{R1(R4+R5)}{R5(2R1+R2)}$	$\frac{-A}{(S^2 + \frac{1}{Q}S + 1)}$
State Variable High-Pass	$\frac{-R2}{R1}$			$\frac{-AS^2}{(S^2 + \frac{1}{Q}S + 1)}$
State Variable Band-Pass	$\frac{R2}{R1}$			$\frac{AS}{(S^2 + \frac{1}{Q}S + 1)}$
Cauer (Elliptical)	$\frac{R2}{R1}$	$F_{Ca} = \frac{200G}{2\pi C1R2}$ $F_{Cb} = \frac{200G}{2\pi C2R2}$		$\frac{R1(R4+R5)}{R5(2R1+R2)}$

The following Figures 6 through 13 illustrate many different filter configurations that are possible with the SSI2140. For each filter type, the table below gives the design equations for gain ("A"), cutoff frequency ("F<sub>c</sub>"), resonance ("Q"), and the transfer functions in terms of "S", where  $S = jf/F_c$ .

Three basic blocks – low-pass, high-pass and all-pass – comprise a single transconductance amplifier, a capacitor, and two or three resistors are shown in Figures 6 through 8, together with typical component values.

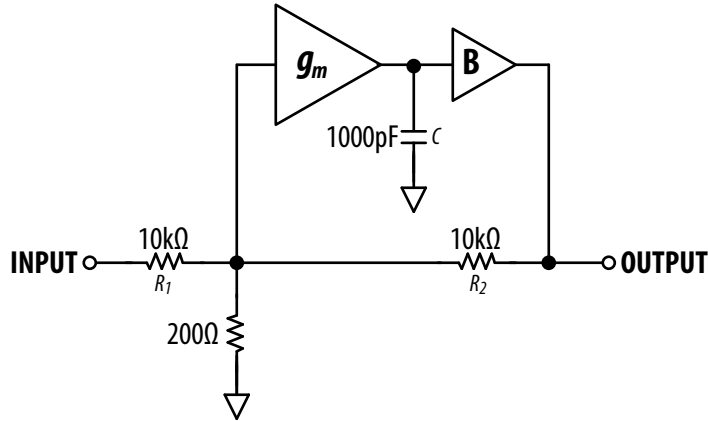


Figure 6: Basic Low-Pass Real Pole Circuit

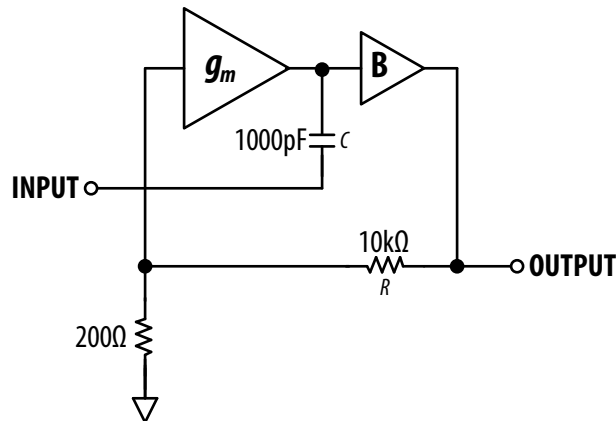


Figure 7: Basic High-Pass Real Pole Circuit

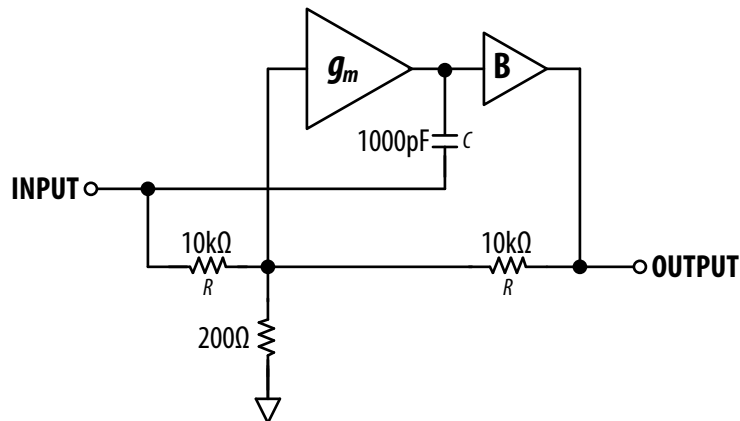
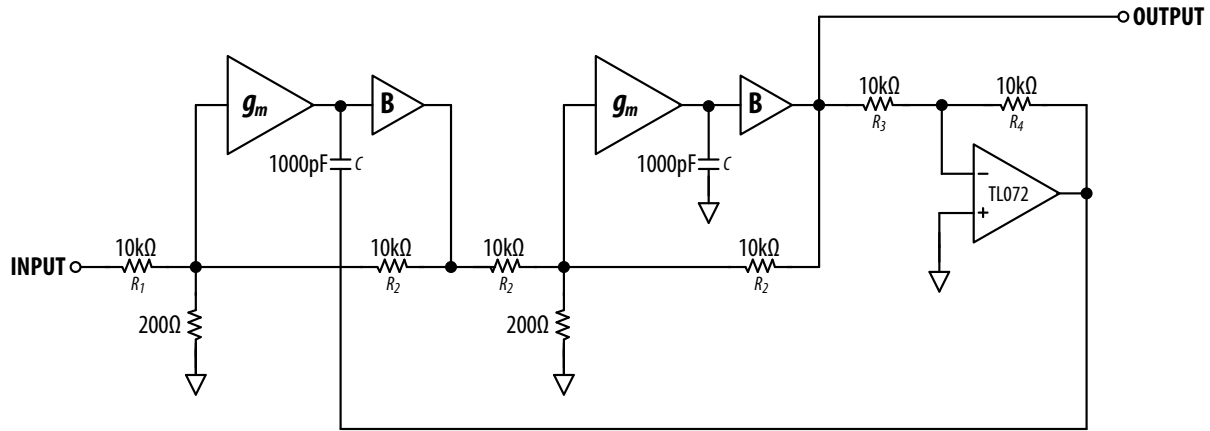
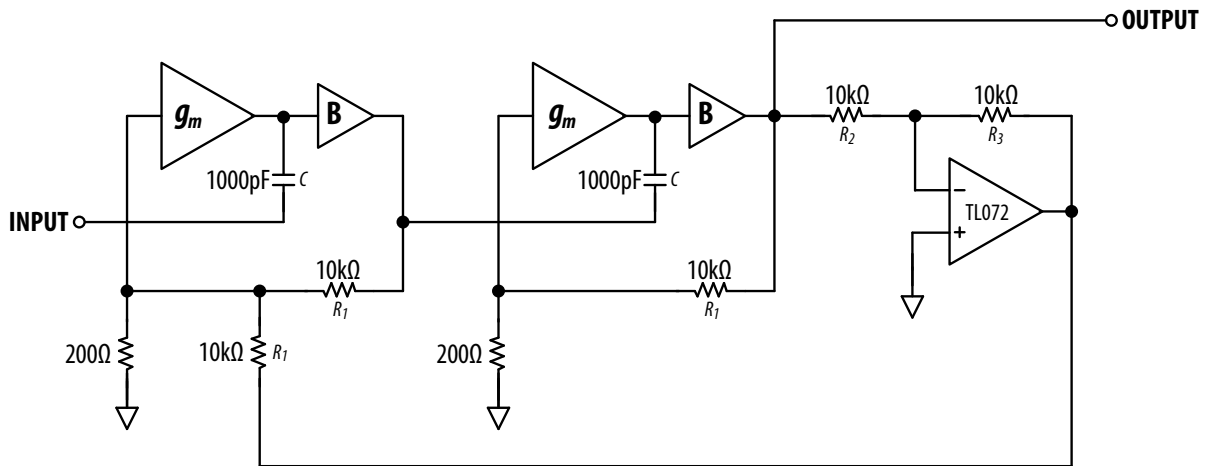


Figure 8: Basic All-Pass Circuit

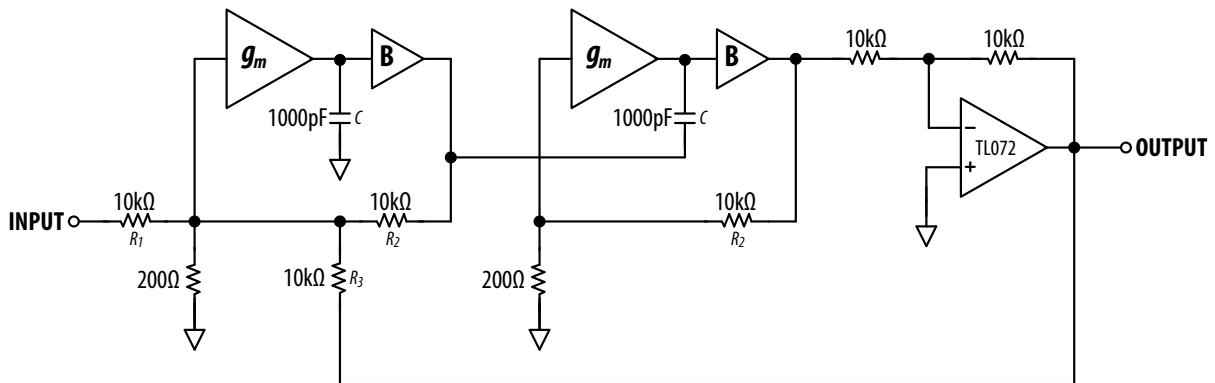
More complex filter schemes are shown in Figures 9 through 12. Two of the most common filter topologies - Sallen and Key and KHN State Variable - are easily realized with the SSI2140 by using two transconductance amplifiers together with an external op-amp.



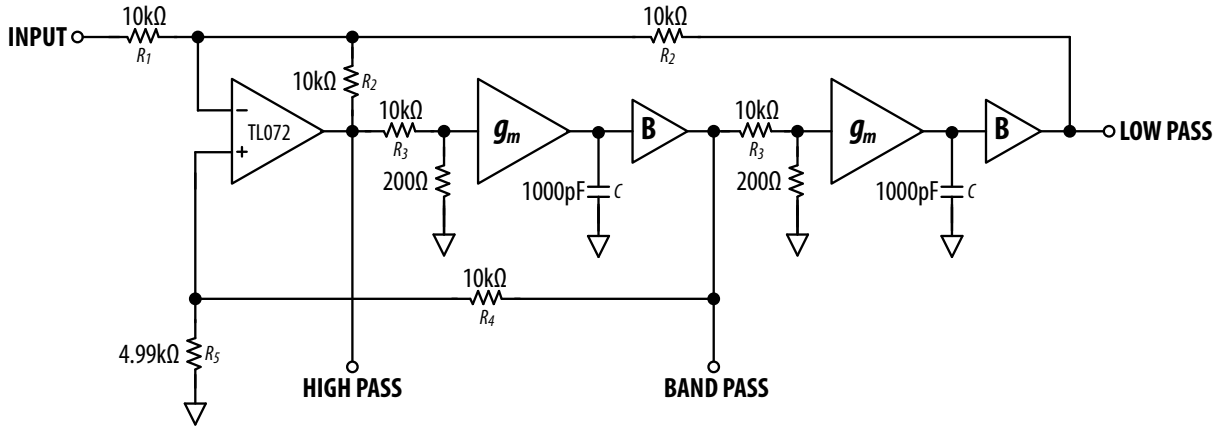
**Figure 9: Sallen and Key Low-Pass Filter**



**Figure 10: Sallen and Key High-Pass Filter**



**Figure 11: Sallen and Key Band-Pass Filter**

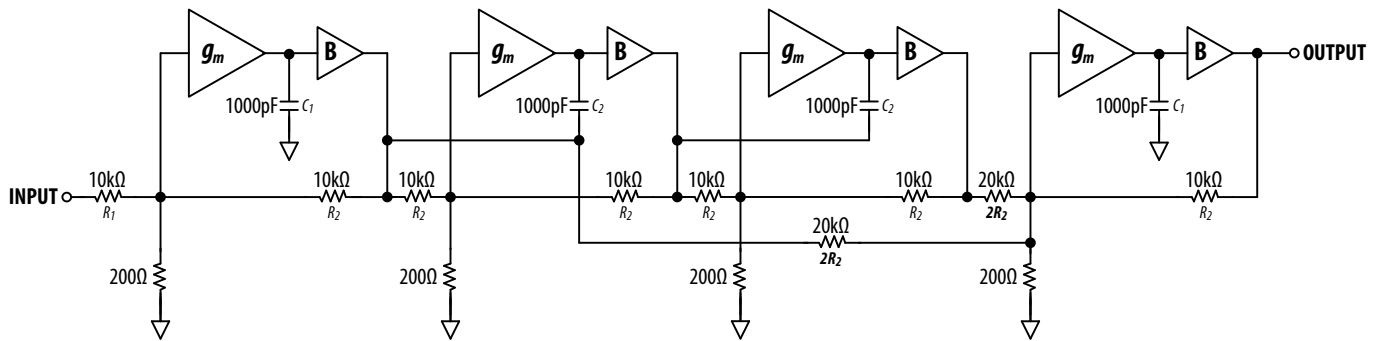


**Figure 12: State Variable Filter**

In order for the State Variable to behave according to the design equations, the parallel combination of R4 and R5 must equal the parallel combination of R1 and R2/2. In algebraic terms:

$$\frac{R4R5}{R4 + R5} = \frac{R1R2}{2R1 + R2}$$

A final example is the Cauer, or Elliptical, filter (Figure 13) giving equalized ripple in the pass and stop bands, and very sharp transition between the passband and stopband. This type is typically used in a DAC reconstruction filter where the sharp cutoff is very close to the ideal brickwall filter needed to get the output bandwidth as close to the Nyquist frequency as possible without sacrificing too much of the high-frequency content.



**Figure 13: Cauer (Elliptical) Filter**

**Q COMPENSATION**

The topology of the Q control circuit determines the type and degree of Q Compensation. Three alternatives are presented. For purposes of clarity the control inputs (Frequency and Q) are not shown as they remain the same in all configurations. If Q compensation is not required, it is possible to use the SSI2140 to implement two filters with a common frequency control, such as a stereo filter or two cascaded filter blocks for sharper cutoff slopes.

**“Classic” Uncompensated Filter**

The configuration of Figure 3 is the simplest, and provides resonance control with no Q compensation. As in the original electronic music four-pole low-pass filter, the passband (DC) gain decreases with increasing Q proportional with gain of the Q VCA. Near oscillation, the passband is attenuated by 12dB.

**Input Gain Compensation**

The Input Gain Compensated configuration of Figure 14 provides Q compensation by feeding the signal input into the positive input of the Q VCA. Thus as the Q increases, more signal is applied to the filter, compensating for the increased negative feedback through the Q VCA. With the values shown, the passband gain remains constant with varying Q. Changing the values of Rqi and Rqg allows the designer to tailor the degree of Q compensation to the particular application. These resistors can also be made variable in real-time by use of a potentiometer or an appropriate VCA. For best Q control rejection, select Rqi to be 16kΩ and Rqg to 1kΩ to match the internal network.

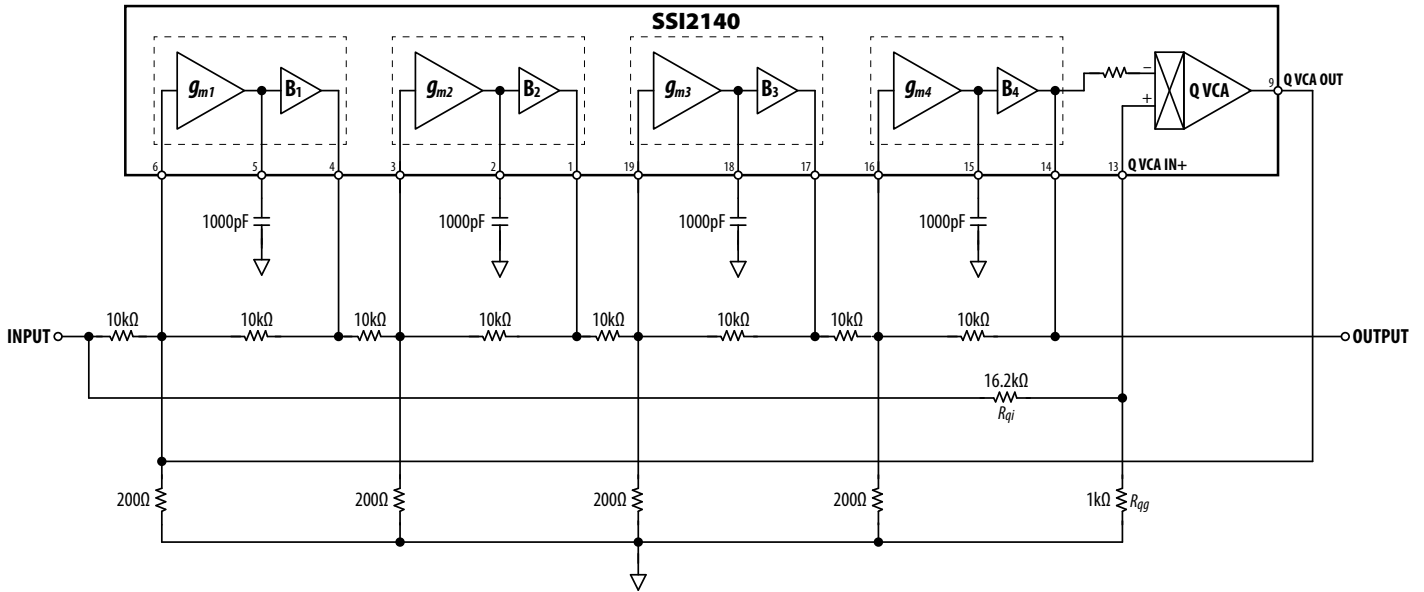


Figure 14: "input Gain" Q Compensation

**Output Gain Compensation**

The Output Gain Compensated configuration of Figure 15 adds compensating gain to the filter core's output to form the final output. In contrast to Input Gain Compensation, the core filter signal level is not altered by Q compensation. This provides less distortion at high Q's resulting in a somewhat different timbre when Q compensation is applied. With the values shown, the passband gain remains constant with varying Q. As above, the various resistor values can be changed to tailor the degree of Q compensation and distortion to the particular application, and can also be made variable in real-time by use of potentiometers or appropriate VCAs.

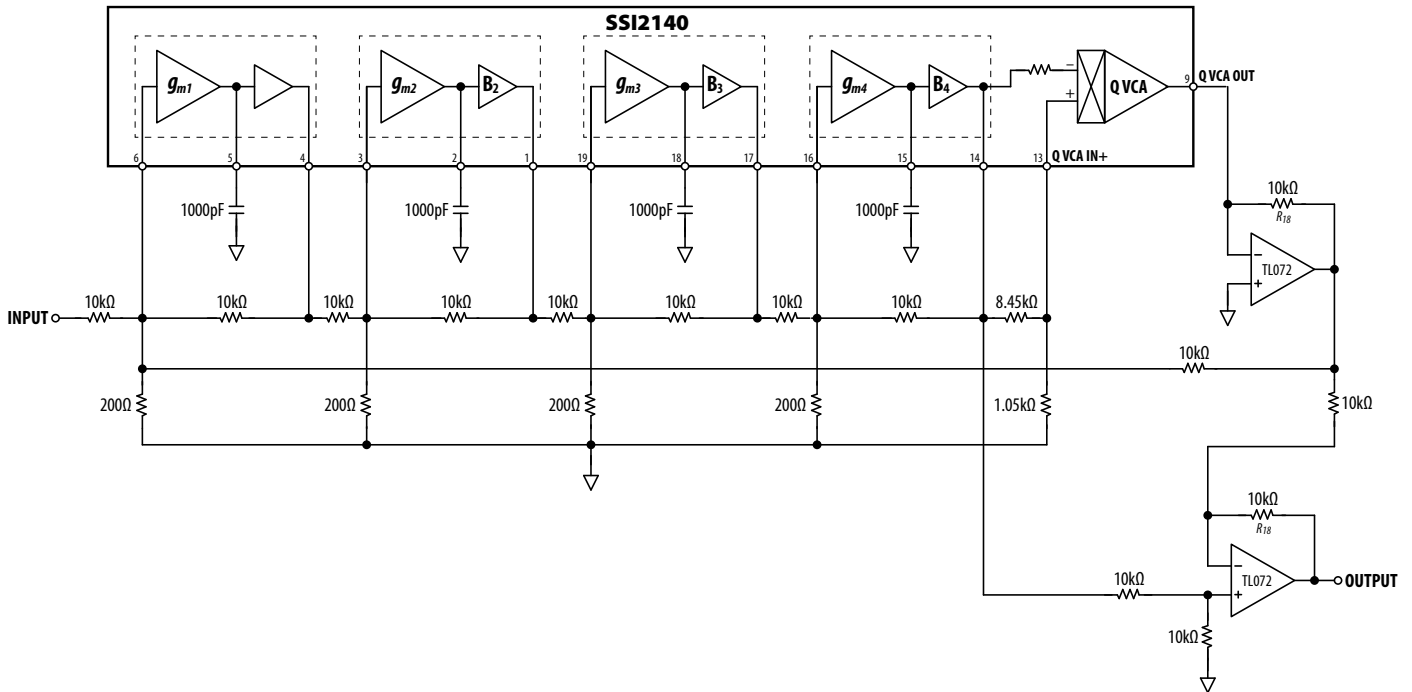


Figure 15: "Output Gain" Q Compensation